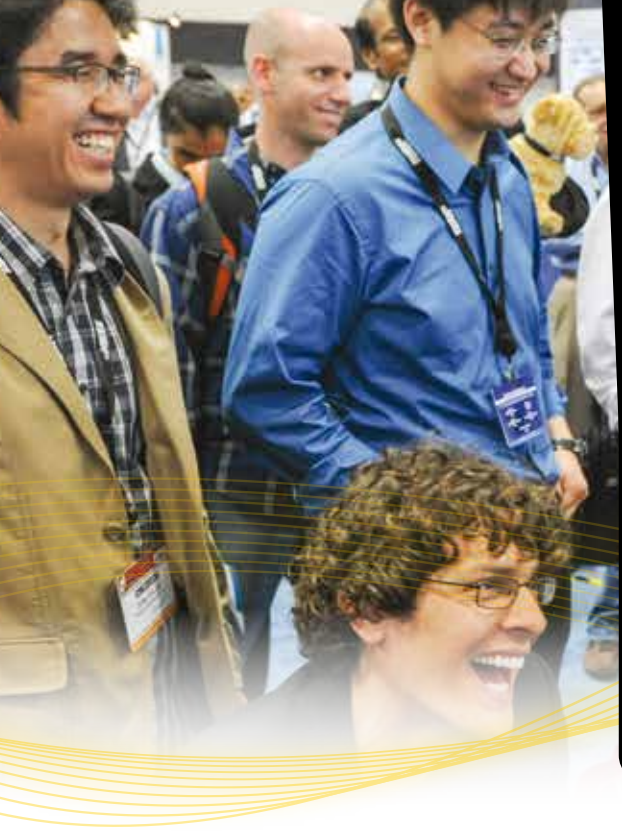

50 YEARS OF INNOVATION

DESIGN AUTOMATION CONFERENCE

CELEBRATING 50 YEARS OF INNOVATION!

FINAL PROGRAM & EXHIBIT GUIDE

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JUNE 2-6, 2013 **AUSTIN CONVENTION CENTER - AUSTIN, TX**

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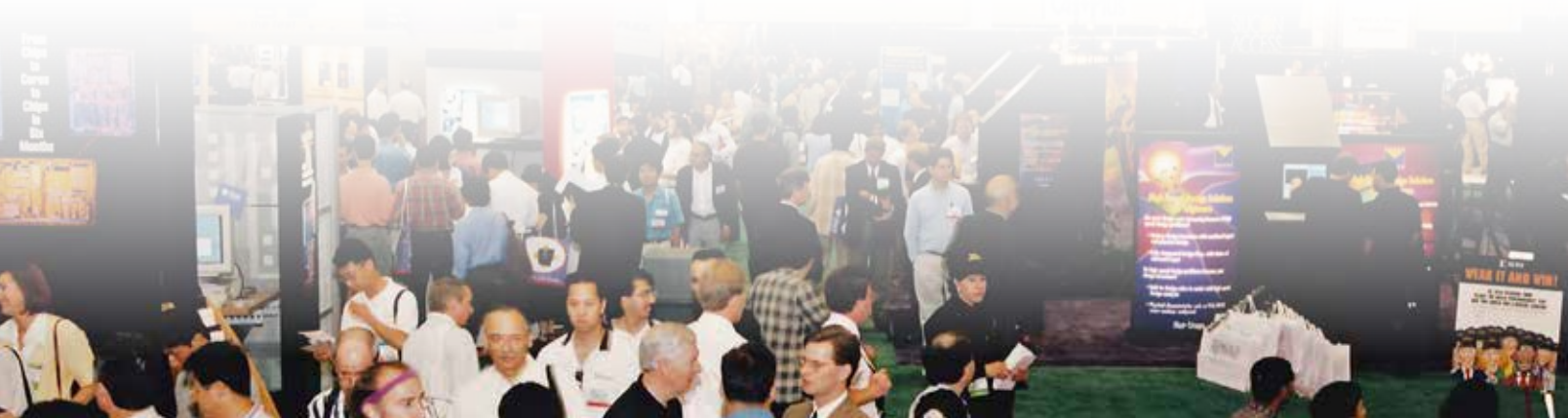

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GENERAL CHAIR WELCOME

Welcome to the 50th DAC

Dear Colleague,

Moving to new design challenges significantly affects the design methodology, flow and suppliers. This year's DAC continues with its mission to play a unique role as an information sharing forum, where the wide range of its offerings allows DAC participants to learn, network and conduct business.

DAC has been evolved from being an EDA conference to becoming more of a design ecosystem conference and extending into design methods, IP, foundries, design services, and Embedded Systems & Software (ESS). More than ever, this year's DAC is pulling together all the above elements of our ecosystem.

The 50th DAC is truly 'grand celebration' with hundreds of paper presentations, vibrant exhibitors, information-packed tutorials, interactive technical and pavilion panels, over 6 focused workshops, an impressive constellation of 6 colocated conferences, and many other novel offerings. The technical program has been designed to optimize personal interactions on all levels. This year's program will include papers from one of our largest pools of submissions (over 740 manuscripts), of which the top 21% have been selected. Of these submissions, more than a third were focused on the ever expanding ESS portion of the conference.

The 50th DAC features a vibrant exhibition showcasing over 175 companies, including the largest EDA vendors, IP providers, ESS suppliers and significant foundries in today's industry. The exhibition will serve as a convenient one-stop-shop for all the elements of the design ecosystem.

The keynotes have been one of the most valuable parts of DAC, leading to our decision to double them for the 50th anniversary. The six speakers will focus on a spectrum of advances in our ecosystem. We will have two CEOs from Austin covering automotive and ESS on Monday, a talk regarding the experiences of a top semiconductor producer on Tuesday, followed by two speakers on Wednesday who will be covering the most recent design trends in the communication domain, and a final keynote about the future of technology, the smart earth.

The Management Day program allows managers and their designers to hear experienced senior managers share their challenges and expertise in management, economics and design optimization.

Designer Track presentations will again be held on the exhibition floor. This track has been created specifically for chip, IP and ESS designers and covers case studies, best practices, methodology, and practical aspects of implementation. This year's track will contain 56 presentations and more than 100 posters, including over 20 presentations dedicated to chips Designed-in-Texas.

A NEW feature at DAC 50 will be our short Visionary Talks, delivered by prominent executives from our EDA/IP community, which will be held during the same plenary sessions as the keynotes. Also new this year are the SKY Talks, which is an abbreviation for Short KeYnotes. The collection of SKY talks, each of which will be 30 minutes, will cover a wide variety of topics with broad appeal. We will also have the Insight Talks presented by DAC's corporate sponsors. Training day at DAC offers attendees the opportunity to attend high-quality training sessions in popular subjects from top training provider Doulos.

In the past 50 years, DAC has helped globalize our industry and wants to continue to do so in the future. To help mark its golden jubilee, the conference will include, beyond this enriched program, a variety of celebratory events. On Monday afternoon, attendees are invited to enjoy an intriguing Global Forum pavilion at the exhibition floor, which will feature dozens of interactive country presentations from all over the globe. Additionally, the mayor of Austin will assist in the opening of Global Forum. On Monday evening, the industry is pooling its resources to hold a lively event at the renowned Austin City Limits, where all DAC attendees and exhibitors are invited. On Wednesday, we will acknowledge the people who made DAC over the last half-century, as authors, exhibitors, and volunteers at our banquet and award ceremony.

Last but not least, I would like to recognize the enormous efforts of the hundreds of dedicated volunteers who made DAC possible by donating their time, expertise, and enthusiasm. Without their hard work and dedication, DAC would not be possible. Please feel free to contact us if you would like to join our exciting team in the future.

DAC is the premier event for networking, where professionals from all over the world converge to sharpen skills, exchange ideas and do business. Join us at the end of each day for a networking reception to unwind, while enjoying the wonderful city of Austin, the capital of live music.

Yervant Zorian
General Chair, 50th DAC

CONFERENCE SPONSORS

ACM

ACM, the Association for Computing Machinery, is the world's largest educational and scientific computing society, uniting computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the computing profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. www.acm.org.

ACM/SIGDA

The ACM Special Interest Group on Design Automation has a long history of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, plus approximately 15 smaller symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the University Booth and Ph.D. Forum at DAC, and the CADathlon at ICCAD, and also funds various scholarships and awards. Other benefits provided to SIGDA members include the SIGDA's E-Newsletter containing information on upcoming conferences and funding opportunities, SIGDA News highlighting most relevant events in EDA and semiconductor industry, and the "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation. For further information on SIGDA's programs and resources, see http://www.sigda.org.

IEEE/COUNCIL ON ELECTRONIC DESIGN AUTOMATION

The IEEE is the world's leading professional association for the advancement of technology, with 400,000 members across 160 countries. The IEEE Council on Electronic Design Automation (CEDA) provides a single focal point for all EDA activities across six major IEEE societies (Circuits & Systems, Computer, Electron Devices, Solid State Circuits, Antennas & Propagation, and Microwave Theory & Techniques). The Council sponsors or co-sponsors over a dozen key EDA conferences, including the Design Automation Conference (DAC), and the International Conference on Computer Aided Design (ICCAD), Design Automation and Test in Europe (DATE) and events at Embedded Systems Week (ESWeek). The Council also publishes the IEEE Transactions on CAD, as well as the IEEE Embedded Systems Letters, and sponsors active technical committees like the DATC and CANDE. Since its founding, the Council has expanded its support of emerging areas within EDA such as nanoscale systems, sponsored new initiatives including the Distinguished Speaker Series and is increasing recognition of members of the EDA profession via awards such as the A. Richard Newton Award, Phil Kaufmann Award, and Early Career Award. The Council welcomes new volunteers and local chapters. For more information on CEDA, visit: www.c-eda.org.

EDA CONSORTIUM

The EDA Consortium (EDAC) is the international association of companies that provide tools and services enabling engineers to create the world's electronic products. EDAC addresses issues that are common to its members and the community they serve. Recent accomplishments include simplification of international EDA export regulation, coordinating software anti-piracy efforts, a quarterly Market Statistics Service (MSS) report, and publication of an industry Operating Systems Roadmap. Companies that become EDAC members are eligible for a 10% discount on DAC Exhibit Booth and Suite Space. Contact the EDA Consortium today about sponsorship and membership opportunities. For more information on the EDA Consortium, visit: www.edac.org.

IMPORTANT INFORMATION

EXHIBIT HOURS

LOCATION: HALLS 1 - 4

HOURS:

Monday, June 3	9:00am - 6:00pm
Tuesday, June 4	9:00am - 6:00pm
Wednesday, June 5	9:00am - 6:00pm

REGISTRATION

LOCATION: SOLAR ATRIUM

HOURS:

Thursday, May 30 - Sunday, June 2	8:00am – 6:00pm
Monday, June 3 - Thursday, June 6	7:00am – 6:00pm

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NEW! ONLINE PROCEEDINGS

For the first time, DAC Proceedings and tutorials will be delivered electronically online via a username and password.

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Password = Registration ID (on your badge)

Please refer to your registration receipt to be reminded of what package and associated files you are eligible to view.

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WIRELESS INTERNET
DAC is offering complimentary wireless internet throughout the Austin Convention Center. Look for:

SSID: DAC2013

MOBILE DEVICES
DAC has a special website built for access from handheld mobile devices. From your smartphone, featurephone, or tablet log in to www.dac.com and you will be automatically redirected to the mobile site. Presentation schedules, the exhibitor listing and other useful information are available and optimized for viewing on small screens.

DAILY UPDATES ON DAC.COM
Check the DAC website daily for a complete listing of each days' schedule, the latest exhibitor announcements, and press coverage. The DAC web site also provides a way to access the proceeding papers on-line.

INFORMATION DESK

The Information Desk is located in the Solar Atrium of the Austin Convention Center.
Dial (512)-404-4600.

"BIRDS-OF-A-FEATHER" MEETINGS

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF). All BOF meetings are held at the Austin Convention Center, Tuesday, June 4 from 7:00 - 8:30pm.

To arrange a BOF meeting, please sign up at the Information Desk located in the Solar Atrium. A meeting room will only be assigned if ten or more people sign up. An LCD projector and screen will be provided.

FIRST AID ROOM

The First Aid Room is located on level one near Hall 3 entrance. A nurse will be on duty at all times while meetings and exhibits are open.

EMERGENCY: 911
Help may be reached 24 hours a day from any house phone within the Austin Convention Center at extension 911.

NETWORKING EVENTS Engage, Meet, Exchange Ideas

WELCOME RECEPTION
Sunday, June 2
Outside Ballroom ABC
5:30 - 7:00pm
Sponsored by: ChipEstimate.com™

GLOBAL FORUM RECEPTION
Monday, June 3
Booth #137
5:00 - 6:00pm
Sponsored by: GLOBALFOUNDRIES, ATIC Advanced Technology Investment Company, A Mubadala Company

KICKIN' IT UP IN AUSTIN
Monday, June 3
AUSTIN CITY LIMITS | 8:00pm - 1:00am

Featuring 9-Time Grammy Award-Winning Band:
ASLEEP AT THE WHEEL

DESIGN AUTOMATION CONFERENCE
CELEBRATING 50 YEARS OF INNOVATION
KICKIN' IT UP IN AUSTIN!
MONDAY, JUNE 3

NETWORKING RECEPTION
Tuesday, June 4
Outside Ballroom ABC
6:00 - 7:00pm

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SPYGLASS, cadence, Mentor Graphics, HEART OF TECHNOLOGY	ChipEstimate.com, Si2, Uniquify	iCScape, JASPER Design Automation, Verilab	AGNISYS, ausdia, CK Design Automation, nimbic, SONICS, REAL INTENT

DAC badge (Conference, Exhibits or Exhibitor) is required for admittance to the event.

WORK-IN-PROGRESS POSTER SESSION & NETWORKING RECEPTION
Wednesday, June 5
Outside Ballroom D
6:00 - 7:00pm

DAC Work-in-Progress (WIP) aims to provide authors an opportunity for early feedback on current work and preliminary results.

LOCATION OF RECEPTIONS:
AUSTIN CONVENTION CENTER

50TH ANNIVERSARY BANQUET
- Special Registration required
Wednesday, June 5
Four Seasons Hotel
7:30pm

NETWORKING RECEPTION
Thursday, June 6
Outside room 11AB
5:30 - 6:30pm

KEYNOTE PRESENTATION

VISIONARY TALK:

WALDEN C. RHINES Chairman and Chief Executive Officer, *Mentor Graphics Corp.*

KEYNOTE:

Embedded Processing – Driving the Internet of Things

GREGG LOWE *Freescale Semiconductor, Inc., Austin, TX*

10:15 — 11:00am

SUMMARY: Embedded processing solutions are the fundamental driver of the emerging Internet of Things, a network of smart devices that will help make our lives easier, safer and more productive. Gregg Lowe will explore the key technology trends that are shaping the global market landscape and examine the application innovations and empowering technologies that are driving today's high-growth market segments.

Our communication networks will be used to connect objects more frequently than connecting people, and embedded systems in automobiles, traffic lights, security systems, appliances, industrial equipment and retail displays will be able to learn, adapt and react to the needs of our everyday lives.

Semiconductor technology will continue to push the limits of integration, bringing together heterogeneous architectures for System-in-Package functionality, and applications will demand more performance and I/O functionality while consuming less power and shrinking into smaller and smaller form factors.

BIO: **Gregg Lowe** was appointed President and CEO of Freescale Semiconductor, effective June 2012. He joined Freescale from Texas Instruments, where he was Senior Vice President, Analog. Gregg joined TI's field sales organization in 1984, with responsibility for growing the company's business with automobile manufacturers. In the early '90s, he led TI's European automotive sales force, managing teams and customer relationships in France, Germany, Italy, England and Spain.

In the mid '90s, Gregg managed TI's Microcontroller organization. Later, he led the Application Specific Integrated Circuit organization for TI, overseeing a worldwide team with design centers and customers in all major regions. In 2001, he moved to the Analog business to manage High Speed Communications and Controls. Later that year, Gregg became manager of the High Performance Analog business unit with responsibility for TI's high-performance data converter, amplifier, power management and interface integrated circuits.

Gregg earned a Bachelor of Science degree in electrical engineering in 1984 from Rose-Hulman Institute of Technology in Terre Haute, Indiana. He later received the university's Career Achievement Award to recognize his accomplishments in the community and within the semiconductor industry. He graduated from the Stanford Executive Program at Stanford University. He is also fluent in German.

Gregg serves as a member of Rose-Hulman Institute of Technology's Board of Trustees. In 2010, the Rock and Roll Hall of Fame and Museum, Inc. in Cleveland, OH, appointed Gregg to its Board of Trustees.

KEYNOTE PRESENTATION

VISIONARY TALK:

LIP-BU TAN President and Chief Executive Officer, *Cadence Design Systems, Inc.*

KEYNOTE:

Looking Ahead to 100 Years – Platform Engineering

JAMES TRUCHARD *National Instruments Corp., Austin, TX*

4:00 — 5:00pm

SUMMARY: Celebrating 50 years of Design Automation Conference is a timely occasion to review the technical and business innovations that have driven the trifecta of higher levels of design abstraction, more prominent software roles, and more cooperative hardware-software design in system development and deployment. Dr. Truchard will share his views on the evolution of traditional and alternative business models in design automation through his unique 37 year perspective as CEO co-founder and visionary leader at National Instruments. The key tenet underlying both Dr. Truchard's and National Instruments' philosophy is a focus on product ecosystem and strong cooperation between hardware and software: a tenet which is becoming increasingly dominant in test, deployment, and design. Dr. Truchard will discuss the benefits of a platform based approach for the design of distributed heterogeneous multicore-processor/FPGA systems. This approach facilitates fast prototyping of applications ranging from advanced control industrial systems to RF and communication systems.

BIO: **Dr. James Truchard** is the co-founder and current president and CEO of National Instruments (NI). Since 1976, he has been leading the vision to equip engineers and scientists with tools that accelerate productivity, innovation, and discovery. Prior to founding National Instruments, Dr. Truchard worked as the director of the Acoustical Measurements Division at the University of Texas Applied Research Laboratory. Dr. Truchard wanted to create a place to work that was fun and provided strong career paths for employees. As he often remarks, "I didn't see a job I wanted in Austin, so I created one!" Dr. Truchard's long-term course for NI balances the successes of its four stakeholders: customers, employees, shareholders, and suppliers. Dr. Truchard and his management team have created an award-winning corporate culture that has been recognized by the Great Place to Work Institute as one of the top 25 "World's Best Multinational Workplaces" and has been on Fortune Magazine's list of "100 Best Companies to Work for in America" for 14 consecutive years.

Dr. Truchard earned his B.S. and M.S. in Physics, and Ph.D. in Electrical Engineering from the University of Texas at Austin. In 1991, Dr. Truchard received the John Fluke Sr. Memorial Award from Test & Measurement World magazine for his significant contributions to the electronics test industry. In 2002, Dr. Truchard was inducted into the Electronic Design Engineering Hall of Fame and he received the Honorary Member Award, the most prestigious award conferred by the Instrumentation, Systems, and Automation society (ISA). He has been a member of the National Academy of Engineering since 2007 and the Royal Swedish Academy of Engineering Sciences since 2003. In 2011, he received the Woodrow Wilson Award for corporate citizenship. Dr. Truchard is dedicated to philanthropy and volunteerism, specifically focusing on education initiatives. Through consistent and collaborative partnerships with organizations including FIRST Robotics, LEGO® Education, and numerous educational non-profits and universities worldwide, he has engaged students with real-world applications and hands-on learning and inspired students to pursue science, technology, engineering and math (STEM) paths.

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GLOBAL FORUM BOOTH #137

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As part of its 50th celebration, DAC honors this geographic breadth and highlights its global reach by organizing a unique and informative venue: the DAC Global Forum (DAC-GF). DAC Global Forum celebrates contributions and future plans of nations around the globe to the field of electronic design in the past 50 years.

Monday, June 3 - 5:00 - 6:00pm

Unveiling Ribbon Cutting Ceremony and Interactive Presentations
Cocktail Hour & Hors d'oeuvres

Welcome Messages from:

Yervant Zorian

Austin Mayor
Lee Leffingwell

Sami Issa

Tuesday, June 4 - 12:00 - 1:30pm & 3:00 - 4:00pm

Interactive presentations

Wednesday, June 5 - 12:15 - 1:30pm & 3:00 - 4:00pm

Interactive presentations

Participating Countries: *as of May 10, 2013*

Armenia	*Italy*	*Morocco*	*Taiwan*
Argentina	*Japan*	*Peru*	*Tunisia*
Brazil	*Jordan*	*Poland*	*Ukraine*
Canada	*Republic of Korea*	*Portugal*	*Uruguay*
China	*Lebanon*	*Russia*	*Vietnam*
Czech Republic	*Lithuania*	*Saudi Arabia*	
Egypt	*Mexico*	*Singapore*	
Estonia	*Malaysia*	*Sweden*	

KEY

Opening Remarks - Yervant Zorian - *50th DAC General Chair*
8:30 - 9:00am

Marie R. Pistilli Women in EDA Achievement Award
For her significant contributions in helping women advance in the field of EDA technology.

Nanette Collins - *NVC Marketing & Public Relations*

P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering
The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African-American, Hispanic, Native American, and physically challenged). In 1989, the ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and a volunteer committee continues to administer the program for DAC. DAC funds a $4000 scholarship, renewable up to five years, to graduating high school seniors.
The 2013 recipient is:

Lynn Hao Thi TRAN

2013 Phil Kaufman Award for Distinguished Contributions to EDA
Dr. Chenming Hu - *TSMC Distinguished Professor of the Graduate School at the University of California, Berkeley*
Dr. Hu is honored for his major contributions to transistor modeling enabling the generation of FinFET based design.

IEEE Council on EDA Distinguished Service Award
For outstanding service and contributions to the IEEE Council on EDA

Rajesh Gupta - *Univ. of California at San Diego*

IEEE Council on EDA Outstanding Service Contribution
For outstanding service to the EDA community as DAC General Chair in 2012

Patrick Groeneveld - *Synopsys, Inc.*

IEEE Fellow
For contributions to design and testing for asynchronous, analog, and genetic circuits

Professor Chris Myers - *Univ. of Utah*

IEEE Fellow
For contributions to design and test of robust integrated circuits

Professor Subhasish Mitra - *Stanford Univ.*

IEEE Fellow
For contributions to VLSI physical design and manufacturability

Yao-Wen Chang - *National Taiwan Univ.*

Donald O. Pederson Best Paper Award for the IEEE Transaction on CAD of Integrated Circuits and Systems
W. Zhang; X. Li, F. Liu, E. Acar, R.A. Rutenbar, R.A., and R.D. Blanton, "Virtual Probe: A Statistical Framework for Low-Cost Silicon Characterization of Nanoscale Integrated Circuits," Vol. 30, Issue: 12, pp. 1814 - 1827, December 2011.

ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation
For seminal work on fast integral equation solvers for integrated circuit parasitic extraction.

Keith Nabors, Jacob White, "FastCap: A Multipole Accelerated 3-D Capacitance Extraction Program," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, November 1991, Vol. 10, Issue 11, Pages 1449-1459.

Keith Nabors - *Apache Design Systems, Ansys Inc.*
Jacob White - *Massachusetts Institute of Technology*

ACM Transactions on Design Automation of Electronic Systems Best Paper Award
For contributions in optimizations techniques for memory design

Jason Cong, W. Jiang, B. Liu and Y. Zou for their paper "Automatic Memory Partitioning and Scheduling for Throughput and Power Optimization," 16(2), April 2011.

Jason Cong - *University of California, Los Angeles*
Wei Jiang - *University of California, Los Angeles*
Bin Liu - *University of California, Los Angeles*
Yi Zou - *University of California, Los Angeles*

ACM-SIGDA Outstanding New Faculty award
In recognition of a junior faculty member who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation.

Shobha Vasudevan - *Assistant Professor, Dept. of Electrical & Computer Engineering, Univ. of Illinois at Urbana-Champaign*

ACM-SIGDA Outstanding Ph.D. Dissertation Award
In recognition of an outstanding Ph.D. dissertation that makes the most substantial contribution to the theory and/or application in the field of electronic design automation.

"CAD for Nanolithography and Nanophotonics"

Duo Ding - *Univ. of Texas at Austin*
David Z. Pan (Advisor) - *Univ. of Texas at Austin*

"Placement and Design Planning for 3D Integrated Circuits"

Guojie Lou - *Univ. of California, Los Angeles*
Jason Cong (Advisor) - *Univ. of California, Los Angeles*

ACM Fellows
To recognize and honor outstanding ACM members for their achievements in computer science and information technology and for their significant contributions to the mission of the ACM.

ACM Fellow
For contributions to physical design automation and to the design for manufacturability of microelectronic systems.

Andrew B. Kahng - *Professor of CSE and ECE*
Univ. of California at San Diego

ACM Fellow
For algorithms for Boolean Satisfiability that advanced the state-of-the-art of hardware verification.

Karem Sakallah - *Professor of EE and CS*
Univ. of Michigan, Ann Arbor

KEYNOTE PRESENTATION

VISIONARY TALK:

AART J. DE GEUS Chairman and co-Chief Executive Officer, *Synopsys, Inc.*

KEYNOTE:

New Challenges for Smarter Mobile Devices

DR. NAMSUNG (STEPHEN) WOO *Samsung, Giheung, Republic of Korea*

9:15 – 10:00am

SUMMARY: EDA technologies and methodologies have been helping design and manufacturing communities of semiconductor industry. Recently, with the rapid growth of mobile applications and smart devices, the EDA community has been focusing on design technologies for low-power and thermal-aware designs. As a result, we now have multiple cases of very powerful mobile application processors which consume only fraction of electrical power compared to traditional processors. We will share some insights and lessons we gained during our pursuit for effective mobile application processors.

Now, the continuing drive for more computing power, lower power consumption and less space to support smarter mobile devices raises new challenges to both design and EDA communities. For some of those challenges (including TSV, FinFet and Packaging), we will present industry perspectives based mostly on our experience at Samsung Semiconductor. We will also demonstrate synergic benefits of collaboration among multiple disciplines at Samsung Semiconductor to address the challenges.

BIO: **Dr. NamSung (Stephen) Woo** is a president of Samsung Electronics and GM of the System LSI business, which consists of three major business areas: SOC, LSI, and ASIC/Foundry. Samsung's System LSI provides industry-leading Application Processors and CMOS image sensors for mobile devices. It also offers cutting-edge technologies (including 28nm HK/MG) for its ASIC/Foundry business. Dr. Woo has given a keynote talk at the CES 2013 in January 2013 and the ISCAS annual conference (sponsored by IEEE) in May 2012. He has published many technical papers and articles in journals and conferences (including DAC), and received a best paper award at the 31st DAC in 1994.

Prior to joining Samsung Electronics in 2004, Dr. Woo has managed engineering and business teams at Texas Instrument, Dot Wireless and Sansearch in San Diego, CA. He also worked at the Bell Laboratories in Murray Hill, New Jersey as a research scientist.

Dr. Woo received Ph.D. in computer science from Univ. of Maryland, College Park, MSEE from KAIST (Korea Advanced Institute of Science and Technology) and BSEE from Seoul National University.

KEY

JOINT KEYNOTE TITLE:
Designing Mobile Communications SoCs: Handhelds to Infrastructure

SUMMARY: The Designer Keynote features leaders from two leading companies in the global wireless communications industry. Scott Runner (Qualcomm) will discuss the interplay between silicon design, power, software, and verification for handheld communications and computing SOCs. Sanjive Agarwala (Texas Instruments) will overview design challenges and solutions for high-performance wireless infrastructure systems. The Designer Keynote will be followed in the afternoon by a special question/answer panel session with Sanjive, Scott, and leads from their design teams.

Design and Methodology of Wireless ICs for Mobile Applications: True SoCs Have Come of Age

J. SCOTT RUNNER *Qualcomm Technologies, Inc., San Diego, CA*

11:15am — 12:15pm

SUMMARY: Today's advanced Systems on a Chip (SoC) for mobile applications are the confluence of high performance CPUs, DSPs, multiple air standard modems for WWAN, WLAN and WPAN, GPS, high end graphics, video and audio CODECs, a variety of peripherals, high speed memory and security and power management technologies on one SoC or SiP. Adding RF, PMIC and DDR memory and you truly have a complete system. Designing such devices marries multiple disciplines of digital and mixed signal HW, SW, systems, design, verification, packaging, physical design engineers and many others. Doing so in the time frames required to satisfy the appetites of smartphone and tablet customers, while delivering to cost, power, performance and quality targets demands novel approaches in design methodology. We will explore methodologies to address HW-SW co-design, power and design verification and validation in the design of the most popular device in the wireless world.

BIO: **Scott Runner** is currently the Vice President of Advanced Methdologies and Low Power Design at Qualcomm Technologies, Inc. He has worked in engineering in the semiconductor and EDA industries for 30 years, holding positions as Director of processors and IP, Design Automation and design manager at Conexant Systems Inc., a "founding" member of the DesignWare team at Synopsys Inc., and DSP and ASIC design engineer and Design Center manager at Fujitsu Microelectronics. He has taped out over 48 devices and has authored over 22 papers & articles. He holds a B.S. in Physics with emphasis in Computer Science and EE from Georgia Tech.

Infrastructure Embedded Processing Systems – Trends and Opportunities

SANJIVE AGARWALA *Texas Instruments, Inc., Dallas, TX*

11:15am — 12:15pm

SUMMARY: The increasingly connected world has created an explosive growth in content creation, distribution and consumption. Embedded systems for infrastructure equipment to handle the content such as wireless base stations, multimedia and video servers, purpose-built servers, medical imaging, and mission critical applications have made great strides in offering unparalleled scale of integration and complete system solutions. Innovations in system and design automation, and semiconductor processing have enabled the industry to deliver flexible and scalable architectures which operators are able to adapt and deploy quickly at impressive cost and performance points. In this talk we will take a closer look at the evolution of the wireless infrastructure market and the enabling system solutions. Wireless operators are seeking cost-effective, high-performance solutions that meet the demands of user traffic today, and position their network architecture for the increased demands of the future. These systems require low-power, high-performance DSP and RISC multicore processing flexibility along with application-specific acceleration, packet processing, networking infrastructure and high bandwidth interfaces all integrated on a single multi-billion transistors Systems-on-Chip. This is all delivered with scalable system architecture in leading-edge semiconductor technologies and software to build complete system solutions. We will examine the progress so far, the trends and opportunities to continue offering value and differentiation to the market.

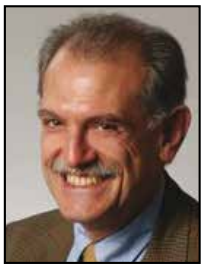
BIO: **Sanjive Agarwala** is a TI Fellow and Director of WW Silicon Development in Processor Business at Texas Instruments. He leads the worldwide development of leading edge SoCs in Communication Infrastructure, Multi-Core DSP, Automotive and Industrial markets at TI. He is also responsible for the roadmap and development of TI C6x DSP core. These arrays of innovative high performance and low power systems are designed in leading edge process technologies with state of the art tools, flows and methodologies. He has worked on a number of generations of high performance DSP/RISC Systems at TI.

Sanjive earned a Master of Science degree in Computer Science in 1989 from Southern Methodist University in Dallas, TX. He also has a Bachelor degree in Electrical Engineering from Punjab Engineering College in India. He is a member of IEEE.

KEYNOTE PRESENTATION

VISIONARY TALK:

KATHRYN KRANEN President and Chief Executive Officer, *Jasper Design Automation, Inc.*



KEYNOTE:

Crystal Ball: From Transistors to the Smart Earth

ALBERTO L. SANGIOVANNI-VINCENTELLI *Univ. of California, Berkeley, CA*

11:00am — 12:00pm

SUMMARY: Design Automation started gaining visibility in the late 1960s when large companies such as IBM and Bell Laboratories were developing new products based on Integrated Circuit technology. The ICs of the time had only a few tens of transistors but the design costs were raising and the need to obtain circuit right the first time became clear. The scientific content of tools and methods for ICs ranged from physics to mathematics in a mix that is rare to see in any other engineering field.

EDA companies have risen and declined, the consideration of the financial community for EDA has been periodically increasing and decreasing, and the algorithms used in EDA have swung from general purpose techniques borrowed from mathematics, computer science, operation research, and artificial intelligence, to ad hoc techniques that leverage the nature of the specific design problem to be solved. Yet, valuable sediment has been deposited by these tides over the years. Progress is achieved when new methodologies crystallize, with new tools and techniques acting as catalysts, that the construction of layers of abstraction are the steps that have helped us reach new heights, that the progress of EDA technology has slowed down just when complexity has reached levels never seen before.

The designer community must leave its traditional shores, under attack by the swarm of killer transistors (more than 1 Billion transistor circuits have been realized), and sail towards a new world where transistors have been tamed. The advances in technology have made it possible to dream about a "smart planet" where trillions of devices are available for humanity.

Design automation and design communities must plan and build together the ships needed to traverse the stormy seas that are facing us in the era of the "Swarm". If we wish to reach the land of opportunity that technology unveils, computer scientist, algorithm designers, MEMS designers, human machine interface experts, biologists, communication system experts, even lawyers and political scientist have to come together if we want that the smart planet be really smart and not a living hell.

BIO: **Alberto Sangiovanni Vincentelli**, Fellow of the IEEE, member of NAE and the Buttner Chair of EECS, University of California, Berkeley, helped founding Cadence and Synopsys, the two largest EDA companies and is a member of the Board of Directors of Cadence, Sonics, KPIT-Cummins and Accent, of the Science and Technology Advisory Board of GM, and of the Technology Advisory Council of UTC. He consulted for major world-wide companies such as IBM, Intel, TI, ST, HP, ATT, Hitachi, Fujitsu, Kawasaki Steel, Telecom Italia, Pirelli, Daimler-Benz, and BMW. He is the President of the Strategic Committee of the Italian Strategic Fund and of the Italian National Council of Research Trustees. He is member of the Executive Committee of the Italian Institute of Technology. He is a member of the Advisory Board of the Lester Center for Innovation of the Haas School of Business and of the Berkeley Roundtable of the International Economy. He is a member of the High-Level Group, of the Steering Committee, of the Governing Board and of the Public Authorities Board of the EU Artemis Joint Technology Initiative. He is member of the Scientific Council of the Italian National Science Foundation.

He received the Kaufman Award for "pioneering contributions to EDA" and the IEEE/RSE Maxwell Medal "for groundbreaking contributions that have had an exceptional impact on the development of electronics and electrical engineering or related fields". He has won 5 best paper awards and a best presentation award at DAC. He is an author of over 880 papers, 17 books and 3 patents.

1 PANEL: ADVANCED NODE RELIABILITY: ARE WE IN TROUBLE?

Room: 16AB
Test and Reliability

TS

As designs move to 20nm and 14nm, reliability issues have become increasingly complex. EM is now a critical design sign-off requirement. ESD failures can significantly degrade the yield. Wear out-related defects impact circuit margining and lifetime requirement for critical applications. This panel will discuss the reliability challenges and debate what would be the best ways for designers, foundries, and EDA vendors to define and develop advanced circuit checks and design sign-off at these advanced nodes.

Moderator:
Andrew Kahng - *Univ. of California at San Diego, La Jolla, CA*

Panelists:
Vassilios Gerousis - *Cadence Design Systems, Inc., San Jose, CA*
Kee Sup Kim - *Samsung, Yongin, Republic of Korea*
Martin Saint-Laurent - *Qualcomm, Inc., Austin, TX*
Michael (Misha) Khazhinsky - *Silicon Laboratories, Inc., Austin, TX*
Valeriy Sukharev - *Mentor Graphics Corp., Freemont, CA*

2 SPECIAL SESSION: MY IP IS BETTER THAN YOURS, BUT DOES ANYONE CARE?

Room: 12AB
System Level Design and Communication

Product differentiation is all the rage. With so many IP components becoming standard, it seems that configurability of IP is the only effective method to allow product designs to differentiate in any significant way. User-driven and provider-offered configurability has become a key advantage in product design. Yet too much configurability makes for enormous design and verification challenges. In this special session, key technical experts from IP providers and integrators will discuss the pros and cons of configurability and answer the question of "how much is enough." Learn how to use your IP most effectively!

Chair:
Norbert Wehn - *Univ. of Kaiserslautern, Kaiserslautern, Germany*

2.1 Goldilocks and the Three Bears of Programmability (10:30am)
Christopher Rowen - *Tensilica, Inc., Santa Clara, CA*

2.2 Challenges of Integrating External IP (11:00am)
Jose Nunez - *Freescale Semiconductor, Inc., Austin, TX*

2.3 SoC Product Differentiation Using Configurable Interconnect IP (11:30am)
Laurent Moll - *Arteris, Inc., Sunnyvale, CA*

3 EMERGING MAPPING AND MANAGEMENT ALGORITHMS FOR PARALLEL EMBEDDED SYSTEMS

Room: 11AB
Embedded Software

The reliance on highly-parallel systems to meet the stringent performance requirements of complex embedded software increases. This session covers the fast-evolving landscape of mapping and resource management algorithms for parallel embedded systems. After an extensive survey and categorization of the research landscape, the session highlights challenges in reliability management for multicore processors, and concludes with important achievements in parallel embedded system modeling.

Chair:
Marco Santambrogio - *Massachusetts Institute of Technology, Cambridge, MA*

3.1 Mapping on Multi/Many-Core Systems: Survey of Current and Emerging Trends (10:30am)
Amit Kumar Singh - *National Univ. of Singapore, Singapore*
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Akash Kumar - *National Univ. of Singapore, Singapore*
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

3.2 Workload and User Experience-Aware Dynamic Reliability Management in Multicore Processors (11:00am)
Pietro Mercati - *Univ. of California at San Diego, La Jolla, CA*
Andrea Bartolini - *Univ. di Bologna, Bologna, Italy*
Francesco Paterna - *Brown Univ., Providence, RI*
Tajana Simunic Rosing - *Univ. of California at San Diego, La Jolla, CA*
Luca Benini - *Univ. di Bologna, Bologna, Italy*

3.3 Liveness Evaluation of a Cyclo-Static DataFlow Graph (11:15am)
Mohamed Benazouz - *CEA-LIST, Gif-sur-Yvette, France*
Alix Munier-Kordon, Thomas Hujsa - *Pierre-and Marie-Curie Univ., Paris, France*
Bruno Bodin - *Kalray Corp., Orsay, France*

▶4 LAY IT OUT, ANALOG!

Room: 13AB
Analog/Mixed-Signal/RF Design

TS

What's up with analog layout? This session focuses on new challenges for emerging analog and mixed-signal (AMS) circuit technologies. The first three papers propose novel physical design solutions for nanoscale AMS circuits that improve printability and matching while reducing coupling. The last paper promotes a new analog neuromorphic computing engine based on memristor for neural network applications.

Chair:
Chenjie Gu - *Intel Corp., Hillsboro, OR*

4.1 Double Patterning Lithography-Aware Analog Placement (10:30am)
Hsing-Chih Chang Chien, Hung-Chih Ou - *National Taiwan Univ., Taipei, Taiwan*
Tung-Chieh Chen, Ta-Yu Kuan - *Synopsys, Inc., Hsinchu, Taiwan*
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

4.2 Simultaneous Analog Placement and Routing with Current Flow and Current Density Considerations (10:45am)
Hung-Chih Ou, Hsing-Chih Chang Chien, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

4.3 Coupling-Aware Length-Ratio-Matching Routing for Capacitor Arrays in Analog Integrated Circuits (11:00am)
Kuan-Hsien Ho, Hung-Chih Ou, Yao-Wen Chang, Hui-Fang Tsao - *National Taiwan Univ., Taipei, Taiwan*

4.4 Digital-Assisted Noise-Eliminating Training for Memristor Crossbar-Based Analog Neuromorphic Computing Engine (11:15am)
Beiye Liu, Miao Hu, Hai Li - *Univ. of Pittsburgh, Pittsburgh, PA*
Tingwen Huang - *Texas A&M Univ., Doha, Qatar*
Wei Zhang - *Nanyang Technological Univ., Singapore*
Zhi-Hong Mao, Yiran Chen - *Univ. of Pittsburgh, Pittsburgh, PA*

▶5 SPECIAL SESSION: DESIGNING AND MODELING BIOLOGY CONTINUES: HURDLES AND PROGRESS

Room: 14
Emerging Design Technologies

Can we design biology like we design circuits? What happens when your genetic circuit is alive and well but evolving over time? A biological circuit is naturally built – now how do I model it? The speakers in this session will provide some answers. The first talk describes why biological parts differ from electronic circuit elements and the challenges faced when designing synthetic gene circuits. The second talk describes how proposed synthetic sequences for designing genetic parts have unintended consequences and the importance of negative design strategies. The last talk proposes a methodology to create discrete models of cell signaling networks and describes its application to the differentiation of immune system cells and malaria effects in mosquito cells.

Chair:
Subarna Sinha - *Stanford Univ., Stanford, CA*

5.1 The Design Problem in Synthetic Biology (10:30am)
Matthew Bennett - *Rice Univ., Houston, TX*

5.2 Negative Design in Synthetic Biology: Refactoring Sequences to Prevent Unwanted Interactions and Evolution (11:00am)
Jeffrey Barrick - *Univ. of Texas at Austin, TX*

5.3 Dynamic Behavior of Cell Signaling Networks - Design and Analysis Automation (11:30am)
Natasa Miskov-Zivanov - *Univ. of Pittsburgh, Carnegie Mellon Univ., Pittsburgh, PA*
Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
James Faeder - *Univ. of Pittsburgh, Pittsburgh, PA*

▶6 TRANSFORMATIONS IN FPGA DESIGN AND PRODUCTIVITY

Room: 15
High-Level and Logic Synthesis

What if the assumptions underlying our FPGA use-model were to suddenly change? This session addresses this question and offers novel solutions to a new design landscape. Cracking the premise of correct underlying circuitry enables nano-scaling to new density ranges. Adaptation of ASIC-style analytic techniques escapes the local-minimum of simulated annealing placement. Tool advances, whether by converting CUDA specifications to FPGA hardware kernels or transforming the logical memory access model into physical FPGA block-RAMs on commercial FPGAs, give a glimpse into the next generation of programmable logic design methodology.

Chair:
Elaheh Bozorgzadeh - *Univ. of California, Irvine, CA*

6.1 Defect Tolerance in Nanodevice-Based Programmable Interconnects: Utilization Beyond Avoidance (10:30am)
Jason Cong, **Bingjun Xiao** - *Univ. of California, Los Angeles, CA*

6.2 An Efficient and Effective Analytical Placer for FPGAs (10:45am)
Tzu-Hen Lin - *National Taiwan Univ., Taipei, Taiwan*
Pritha Banerjee - *Univ. of Calcutta, Kolkata, India*
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

6.3 Throughput-Oriented Kernel Porting onto FPGAs (11:00am)
Alexandros Papakonstantinou, Deming Chen,
Wen-Mei Hwu - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Jason Cong - *Univ. of California, Los Angeles, CA*
Yun Liang - *Peking Univ., Beijing, China*

6.4 Memory Partitioning for Multidimensional Arrays in High-level Synthesis (11:15am)
Yuxin Wang, Peng Li - *Peking Univ., Beijing, China*
Peng Zhang - *Univ. of California, Los Angeles, CA*
Chen Zhang - *Peking Univ., Beijing, China*
Jason Cong - *Univ. of California, Los Angeles, CA*

7 PANEL: I BLEW MY POWER BUDGET: WHOM SHOULD I THROW UNDER THE BUS?

Room: 16AB
Low-Power Design and Power Analysis

TS

During the last phases of the design, or even after first silicon, I discover that the power budget is blown. What can I do at this point? Whom do I blame? What should I do to ensure this does not happen again? The panelists will tell their horror tales. Let's see who gets thrown under the bus…

Moderator:
John Donovan - *Low-PowerDesign.com, Austin, TX*

Panelists:
Clive Bittlestone - *Texas Instruments, Inc., Dallas, TX*
Rick Hofmann - *Qualcomm Technologies, Inc., Raleigh, NC*
Anis Jarrar - *Freescale Semiconductor, Inc., Austin, TX*
Arvind Shanmugavel - *Apache Design, Inc. a subsidiary of ANSYS, Inc., Canonsburg, PA*

SESSION 13: SKY TALK: 2:30 - 3:00PM
Post-Exponential Innovation

8 SPECIAL SESSION: BALANCING SECURITY AND UTILITY IN MEDICAL DEVICES

Room: 12AB
Security

Medical Devices, both implanted and wearable, are increasingly being used to solve a wide variety of medical and research challenges. However, they introduce potential vulnerabilities to adversaries that can result in life-threatening situations as well as compromises of privacy. There is a tension between the security and usability of the device for legitimate purposes. These challenges are greatly dependent on the design of the underlying electronics and wireless communications. This is an increasingly cross-disciplinary topic between the Security and Design communities. Issues include low-power/energy design, wireless, cross-layer threats, energy harvesting, and sensors.

Chair:
Farinaz Koushanfar - *Rice Univ., Houston, TX*

8.1 Balancing Security and Utility in Medical Devices? (1:30pm)
Farinaz Koushanfar - *Rice Univ., Houston, TX*
Wayne Burleson - *Univ. of Massachusetts, Amherst, MA*
Masoud Rostami - *Rice Univ., Houston, TX*
Ari Juels - *RSA Labs, Cambridge, MA*

8.2 Secure Embedded Software for Medical Devices (1:45m)
Kevin Fu - *Univ. of Michigan, Ann Arbor, MI*

8.3 Meeting Security Requirements in Medical Devices (2:00pm)
Ken Hoyme - *Boston Scientific Corp., Twin Cities, MN*

8.4 Towards Trustworthy Medical Devices and Body Area Networks (2:15pm)
Anand Raghunathan - *Purdue Univ., West Lafayette, IN*
Niraj Jha, Meng Zhang - *Princeton Univ., Princeton, NJ*

8.5 Low-Energy Encryption for Medical Devices: Security Adds an Extra Design Dimension (2:30pm)
Ingrid Verbauwhede, Vladimir Rožić, Oscar Reparaz, Junfeng Fang - *Katholieke Univ. Leuven, Belgium*

9 TEACHING THE OLD BACKEND COMPILER DOG NEW TRICKS

Room: 11AB
Embedded Software

Reliability and energy-efficiency constraints create new expectations for embedded system compilers. Meeting these expectations requires new advances on optimization techniques for instruction-level parallelism and new research on reliability- and resource-aware code mappings. Learn about the new and exciting directions in compilers.

Chair:
Gert Goossens - *Target Compiler Technologies, Leuven, Belgium*

9.1 Aging-Aware Compiler-Directed VLIW Assignment for GPGPU Architectures (1:30pm)
Abbas Rahimi - *Univ. of California at San Diego, La Jolla, CA*
Luca Benini - *Univ. di Bologna, Bologna, Italy*
Rajesh Gupta - *Univ. of California at San Diego, La Jolla, CA*

9.2 Exploiting Program-Level Masking and Error Propagation for Constrained Reliability Optimization (1:45pm)
Muhammad Shafique, Semeen Rehman, Pau Vilimelis Aceituno, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

9.3 REGIMap: Register-Aware Application Mapping on Coarse-Grained Reconfigurable Architectures (CGRAs) (2:00pm)
Mahdi Hamzeh, Aviral Shrivastava, Sarma Vrudhula - *Arizona State Univ., Tempe, AZ*

9.4 Polyhedral Model Based Mapping Optimization of Loop Nests for CGRAs (2:15pm)
Dajiang Liu, Shouyi Yin, Leibo Liu, Shaojun Wei - *Tsinghua Univ., Beijing, China*

10 ANSWERS TO SOME OF YOUR EMBEDDED SYSTEM DESIGN QUESTIONS

Room: 13AB
Embedded Design Methodologies

TS

You've got questions about embedded systems design? Our speaker have answers! Approximate microarchitecture computations offer energy efficiency. But, what about errors? Instruction set simulators are critical for architecture design and system exploration. But, how do you improve their speed? Last level cache access patterns have profound impact on DRAM power. But, how do you drive your cache optimization in the presence of DRAM process variations?

Chair:
Philip Brisk - *Univ. of California, Riverside, CA*

10.1 Improving Energy Gains of Inexact DSP Hardware Through Reciprocative Error Compensation (1:30pm)
Avinash Lingamneni - *Rice Univ., Houston, TX*
Arindam Basu - *Nanyang Technological Univ., Singapore*
Christian Enz - *Centre Suisse d'Electronique et Microtechnique SA, Neuchatel, Switzerland*
Krishna Palem - *Rice Univ., Houston, TX*
Christian Piguet - *Centre Suisse d'Electronique et Microtechnique SA, Neuchatel, Switzerland*

10.2 Early Partial Evaluation in a JIT-compiled, Retargetable Instruction Set Simulator Generated from a High-Level Architecture Description (1:45pm)
Harry Wagstaff, Miles Gould, Björn Franke, Nigel Topham - *Univ. of Edinburgh, Edinburgh, United Kingdom*

10.3 XDRA: Exploration and Optimization of Last-Level Cache for Energy Reduction in DDR DRAMs (2:00pm)
Su Myat Min, Haris Javaid, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

10.4 Towards Variation-Aware System-Level Power Estimation of DRAMs: An Empirical Approach (2:15pm)
Karthik Chandrasekar - *Delft Univ. of Technology, Eindhoven, The Netherlands*
Christian Weis - *Technische Univ. Kaiserslautern, Kaiserslautern, Germany*
Benny Akesson - *Polytechnic Institute of Porto, Portugal*
Norbert Wehn - *Technische Univ. Kaiserslautern, Kaiserslautern, Germany*
Kees Goossens - *Technische Univ. Eindhoven, Eindhoven, The Netherlands*

11 DON'T FRET ABOUT YOUR FINFET: PHYSICAL DESIGN IN 14NM AND BEYOND

Room: 14
Physical Design

Technology scaling into the 14nm node and beyond brings many new challenges to physical design algorithms and optimization. In this new world, FinFet devices, E-Beam lithography, design rule corrections and 3D design planning are all essential to succeeding designing in advance technology nodes. Put your fears aside in this session as you learn about techniques for addressing these modern physical design challenges.

Chair:
Huang-Yu Chen - *Taiwan Semiconductor Manufacturing Co., Ltd., San Francisco, CA*

11.1 TEASE: A Systematic Analysis Framework for Early Evaluation of FinFET-based Advanced Technology Nodes (1:30pm)
Arindam Mallik, Paul Zuber, Tsung-Te Liu, Bharani Chava, Bhavana Ballal, Pablo Del Barrio, Rogier Baert, Kris Croes, Julien Ryckaert, Mustafa Badaroglu, Abdelkarim Mercha, Diederik Verkest - *IMEC, Leuven, Belgium*

11.2 Stitch-Aware Routing for Multiple E-Beam Lithography (1:45pm)
Shao-Yun Fang, Iou-Jen Liu, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

11.3 Automatic Design Rule Correction in Presence of Multiple Grids and Track Patterns (2:00pm)
Nitin Salodkar, Subramanian Rajagopalan, Sambuddha Bhattacharya, Shabbir Batterywala - *Synopsys (India) Pvt. Ltd., Bangalore, India*

11.4 Multiple Chip Planning for Chip-Interposer Codesign (2:15pm)
Yuan-Kai Ho, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

12 TAMING THE BEAST: COPING WITH IMPERFECT DESIGN AND SILICON DEFECTS

Room: 15
Test and Reliability

Bug-free design and defect-free fabrication are nearly impossible. Design and silicon imperfections are exposed using a parallelized test generation algorithm, a virtual machine-based silicon validation, and elegant approaches for isolating defects in test-access and error-recovery logic.

Chair:
Steve Palosh - *Freescale Semiconductor, Inc., Austin, TX*

12.1 GPU-Based N-Detect Transition Fault ATPG (1:30pm)
Kuan-Yu Liao, Sheng-Chang Hsu, James C-M Li - *National Taiwan Univ., Taiwan, Taiwan*

12.2 Post-Silicon Conformance Checking with Virtual Prototypes (1:45pm)
Li Lei, Fei Xie, Kai Cong - *Portland State Univ., Portland, OR*

12.3 On Testing Timing-Speculatative Circuits (2:00pm)
Feng Yuan, Yannan Liu - *The Chinese Univ. of Hong Kong, Hong Kong*
Wen-Ben Jone - *Univ. of Cincinnati, Cincinnati, OH*
Qiang Xu - *The Chinese Univ. of Hong Kong, , Hong Kong*

12.4 An ATE Assisted DFD Technique for Volume Diagnosis of Scan Chains (2:15pm)
Subhadip Kundu, Santanu Chattopadhyay, Indranil Sengupta - *Indian Institute of Technology, Kharagpur, India*
Rohit Kapur - *Synopsys, Inc., Mountain View, CA*

14 PANEL: IS SECURITY THE NEXT DESIGN DIMENSION?

Room: 16AB
Security

TS

Vulnerabilities in many embedded systems including cars, voting machines, medical devices, etc. have been recently demonstrated. These incidents raise an important question - how should security be considered during the design phase? It is well-known that incorporating security late in a design is a recipe for disaster (e.g. the Internet). But how should security be prioritized with other design criteria like cost, power, and reliability. At what point can threats be modeled and defenses defined. The panel will discuss the vulnerabilities in integrated circuits and embedded systems and potential solutions to building-in security during design.

Moderator:
Wayne Burleson - *Univ. of Massachusetts, Amherst, MA*

Panelists:
Srini Devadas - *Massachusetts Institute of Technology, Cambridge, MA*
Kevin Gotze - *Intel Corp., Hillsboro, OR*
Kevin Fu - *Univ. of Michigan, Ann Arbor, MI*
Saverio Fazzari - *Booz Allen Hamilton, Inc., Arlington, VA*

SESSION 20: SKY TALK: 5:30 - 6:00PM
What a Chip Designer Needs at the End of Moore's Law

15 SPECIAL SESSION: THE SILICON FLASHLIGHT: MAPPING THE ROAD TO 6NM

Room: 12AB
General Interest

Is the Yellow Brick Road on Google Maps? If it were, would we be able to follow it? For a long time, the International Technology Roadmap for Semiconductors (ITRS) has been "the" blueprint for the future of Silicon technology. But this was in a world where the industry moved forward as one to each progressively finer geometry. Today, it is clear to all that the Moores Law Locomotive has slowed down dramatically in the last few years. A lot of consolidation has happened and many Silicon fabricators have stopped scaling altogether, choosing to rely on foundry services for the few devices where the latest and greatest technology is required. At a time of increased uncertainty, mounting lithographic challenges, and reduced R&D investment, knowing what the future of technology holds can be difficult for design teams trying to create product roadmaps. It is of paramount importance that design teams understand how these roadmaps are created, how reliable the predictions are, and how to use other sources of predictive information to extend or verify the roadmap.

Chair:
Kevin Cao - *Arizona State Univ., Tempe, AZ*

15.1 Mapping Silicon Roadmaps to Product Roadmaps (4:00pm)
Ghavam Shahidi - *IBM Corp., Yorktown Heights, NY*

15.2 Predicting Future Technology Performance (4:30pm)
Asen Asenov, Craig Alexander - *Gold Standard Simulations Ltd., Glasgow, United Kingdom*
Craig Riddet, Ewan Towie - *Univ. of Glasgow, Glasgow, United Kingdom*

15.3 Predicting Future Product Performance: Modeling and Evaluation of Standard Cells in FinFET Technologies (5:00pm)
Ulf Schlichtmann, Veit Kleeberger, Helmut Graeb - *Technical Univ. of Munich, Munich, Germany*

15.4 The ITRS Process and Current Status (5:30pm)
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

16 BETTER TO BE PROACTIVE OR BE A SLACKER IN NOC DESIGN?

Room: 11AB
System Level Design and Communication

As we roll out the red carpet for state-of-the-art network-on-chip designs, our speakers explore proactive, agile, and relaxed methods to improve performance in future many core systems. Even the session's "slackers" have something to contribute by minimizing rising energy requirements in networks-on-chip through local and global bandwidth analyses. Our "geriatric" specialist concludes the session with a mechanism to deal with aging phenomena in networks-on-chip.

Chair:
Sudeep Pasricha - *Colorado State Univ., Fort Collins, CO*

16.1 Proactive Circuit Allocation in Multiplane NoCs (4:00pm)
Ahmed Abousamra, Alex Jones, Rami Melhem - *Univ. of Pittsburgh, Pittsburgh, PA*

16.2 A Heterogeneous Multiple Network-on-Chip Design: An Application-Aware Approach (4:15pm)
Asit Mishra - *Intel Corp., Hillsboro, OR*
Onur Mutlu - *Carnegie Mellon Univ., Pittsburgh, PA*
Chita Das - *Pennsylvania State Univ., University Park, PA*

16.3 Designing Energy-Efficient NoC for Real-Time Embedded Systems Through Slack Optimization (4:30pm)
Jia Zhan - *Pennsylvania State Univ., University Park, PA*
Nikolay Stoimenov - *Eidgenössische Technische Hochschule Zürich, Zurich, Switzerland*
Jin Ouyang - *NVIDIA Corp., Santa Clara, CA*
Lothar Thiele - *Eidgenössische Technische Hochschule Zürich, Zurich, Switzerland*
Vijaykrishnan Narayanan - *Pennsylvania State Univ., University Park, PA*
Yuan Xie - *Pennsylvania State Univ., Advanced Micro Devices, Inc., University Park, PA*

16.4 RISO: Relaxed Network-on-Chip Isolation for Cloud Processors (4:45pm)
Hang Lu, Guihai Yan, Yinhe Han, Binzhang Fu, Xiaowei Li - *Chinese Academy of Sciences, Beijing, China*

16.5 Smart Hill Climbing for Agile Dynamic Mapping in Many-Core Systems (5:00pm)
Mohammad Fattah, Masoud Daneshtalab, **Pasi Liljeberg**, Juha Plosila - *Univ. of Turku, Turku, Finland*

16.6 HCI-Tolerant NoC Router Microarchitecture (5:15pm)
Dean Ancajas, James McCabe Nickerson, Koushik Chakraborty, Sanghamitra Roy - *Utah State Univ., Logan, UT*

▶17 OFF-THE-SHELF TECHNIQUES FOR QUANTUM AND BIO CIRCUITS

Room: 13AB
Emerging Design Technologies

TS

Everything old is new again. In this session you will learn how established approaches in EDA are being applied to new and emerging design technologies. As examples, graph theory is used to estimate the run times of quantum programs. Additionally, techniques used to study process variability and multi-objective function optimization are applied to biological networks. Finally, frequency scaling is applied in the design of cyperphysical microfluidic biochips.

Chair:
Smita Krishnaswamy - *Columbia Univ., New York, NY*

17.1 Optimization of Quantum Circuits for Interaction Distance in Linear Nearest Neighbor Architectures (4:00pm)
Alireza Shafaei, Mehdi Saeedi, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

17.2 LEQA: Latency Estimation for a Quantum Algorithm Mapped to a Quantum Circuit Fabric (4:15pm)
Mohammad Javad Dousti, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

17.3 Pareto epsilon-Dominance and Identifiable Solutions for BioCAD Modeling (4:30pm)
Claudio Angione - *Univ. of Cambridge, United Kingdom*
Jole Costanza, Giovanni Carapezza - *Univ. degli Studi di Catania, Catania, Italy*
Pietro Liò - *Univ. of Cambridge, Cambridge, United Kingdom*
Giuseppe Nicosia - *Univ. degli Studi di Catania, Catania, Italy*

17.4 Design of Cyberphysical Digital Microfluidic Biochips under Completion-Time Uncertainties in Fluidic Operations (4:45pm)
Yan Luo, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Tsung-Yi Ho - *National Cheng Kung Univ., Tainan City, Taiwan*

17.5 Gene Modification Identification under Flux Capacity Uncertainty (5:00pm)
Mona Yousofshahi - *Tufts Univ., Medford, MA*
Michael Orshansky - *Univ. of Texas at Austin, TX*
Kyongbum Lee, **Soha Hassoun** - *Tufts Univ., Medford, MA*

17.6 A Field-Programmable Pin-Constrained Digital Microfluidic Biochip (5:15pm)
Daniel Grissom, Philip Brisk - *Univ. of California, Riverside, CA*

▶18 ENLARGING THE UNIVERSE: INNOVATIVE EXPLORATION FOR RTL AND HIGH-LEVEL SYNTHESIS

Room: 14
High-Level and Logic Synthesis

This session explores new ways of charting the logic- and high-level synthesis universe, to direct EDAtools to better explore the design space. Several approaches open new doors for domain-specific problems, finding systematic techniques to identify Pareto-optimal implementations, ranging from high-performance prefix adders, to feedback decoders, to iterative stencil loop algorithms used for streaming applications. In addition, challenging and potent optimization techniques, based on majority decomposition, are introduced into a logic synthesis tool. Finally, machine learning and runtime dependency analysis techniques are proposed to venture into hard-to-reach corners of the design space.

Chair:
Sunil Khatri - *Texas A&M Univ., College Station, TX*

18.1 BDS-MAJ: A BDD-Based Logic Synthesis Tool Exploiting Majority Logic Decomposition (4:00pm)
Luca Amaru, Pierre-Emmanuel Gaillardon, Giovanni De Micheli - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*

18.2 Towards Optimal Performance-Area Trade-Off in Adders by Synthesis of Parallel Prefix Structures (4:15pm)
Subhendu Roy - *Univ. of Texas at Austin, TX*
Mihir Choudhury, Ruchir Puri - *IBM T.J. Watson Research Center, Yorktown Hts, NY*
David Pan - *Univ. of Texas at Austin, TX*

18.3 Synthesis of Feedback Decoders for Initialized Encoders (4:30pm)
Kuan-Hua Tu, Jie-Hong Roland Jiang - *National Taiwan Univ., Taipei, Taiwan*

18.4 On Learning-Based Methods for Design-Space Exploration with High-Level Synthesis (4:45pm)
Hung-Yi Liu, Luca Carloni - *Columbia Univ., New York, NY*

18.5 Runtime Dependency Analysis for Loop Pipelining in High-Level Synthesis (5:00pm)
Mythri Alle - *Univ. de Rennes 1, Rennes, France*
Antoine Morvan - *INRIA, Rennes, France*
Steven Derrien - *Univ. de Rennes 1, Rennes, France*

18.6 A High-Level Synthesis Flow for the Implementation of Iterative Stencil Loop Algorithms on FPGA Devices (5:15pm)
Alessandro Antonio Nacci, Vincenzo Rana - *Politecnico di Milano, Milan, Italy*
Ivan Beretta - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*
Francesco Bruschi - *Politecnico di Milano, Milan, Italy*
David Atienza - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*
Donatella Sciuto - *Politecnico di Milano, Milan, Italy*

19 EMERGING APPLICATION-ORIENTED, LOW-POWER TECHNIQUES

Room: 15
Low-Power Design and Power Analysis

TS

Low power requirements have become ubiquitous and have emerged in very diverse contexts that have not been traditionally power-oriented. The papers in this session present novel technologies that achieve low power. The target applications include memory of ultra-high data storage density, hardware-assisted watchpoint systems, energy harvesting embedded systems, MIMO RF transceiver systems, and network on chip. In these applications, state-of-the-art technologies expanding from circuit to system level are utilized and significant power saving is demonstrated by these papers.

Chair:
Iris Bahar - *Brown Univ., Providence, RI*

19.1 Cross-Layer Racetrack Memory Design for Ultra High Density and Low Power Consumption (4:00pm)
Zhenyu Sun - *Univ. of Pittsburgh, Pittsburgh, PA*
Wenqing Wu - *Qualcomm Technologies, Inc., San Diego, CA*
Hai Li - *Univ. of Pittsburgh, Pittsburgh, PA*

19.2 Improving the Energy Efficiency of Hardware-Assisted Watchpoint Systems (4:15pm)
Vasileios Karakostas - *Barcelona Supercomputing Center and Univ. Politecnica de Catalunya, Barcelona, Spain*
Sasa Tomic, Osman Unsal, Mario Nemirovsky - *Barcelona Supercomputing Ctr., Barcelona, Spain*
Adrian Cristal - *Barcelona Supercomputing Center and IIIA-CSIC, Barcelona, Spain*

19.3 Low-Power Area-Efficient Large-Scale IP Lookup Engine Based on Binary-Weighted Clustered Networks (4:30pm)
Naoya Onizawa, **Warren Gross** - *McGill Univ., Montreal, QB, Canada*

19.4 Real-Time Use-Aware Adaptive MIMO RF Receiver Systems for Energy Efficiency Under BER Constraints (4:45pm)
Debashis Banerjee, Shyam Devarakond - *Georgia Institute of Technology, Atlanta, GA*
Shreyas Sen - *Intel Corp., Atlanta, GA*
Abhijit Chatterjee - *Georgia Institute of Technology, Atlanta, GA*

19.5 Improving Charging Efficiency with Workload Scheduling in Energy Harvesting Embedded Systems (5:00pm)
Yukan Zhang, Yang Ge, Qinru Qiu - *Syracuse Univ., Syracuse, NY*

19.6 Creation of ESL Power Models for Communication Architectures using Automatic Calibration (5:15pm)
Stefan Schürmans, Diandian Zhang, Dominik Auras, Rainer Leupers, Gerd Ascheid - *RWTH Aachen Univ., Aachen, Germany*
Xiaotao Chen, Lun Wang - *Huawei Technologies Co., Ltd., Plano, TX*

21 PANEL: DISRUPTIVE VERIFICATION TECHNOLOGIES: CAN THEY REALLY MAKE A DIFFERENCE?

Room: 16AB
Verification and Simulation

TS

Common wisdom is that there is no disruptive technology on the horizon to address the looming verification crisis. Indeed, most verification teams remain too busy, understaffed and barely able to keep pace with the innovation in design. But there is hope. For those who see nothing, the panel will illuminate. Those who don't trust anything but the status quo will have an opportunity to debate and air their concerns. Come listen and debate the most promising technologies and how best should they be adopted for industrial use.

Moderator:
Brian Bailey - *Brian Bailey Consulting, Beaverton, OR*

Panelists:
Ken Albin - *Intel Corp., Austin, TX*
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*
John Goodenough - *ARM, Ltd., San Jose, CA*
Adnan Hamid - *Breker Verification Systems, Inc., San Jose, CA*
Alan Hu - *Univ. of British Columbia, Vancouver, BC, Canada*
Ziyad Hanna - *Jasper Design Automation, Inc., Haifa, Israel*

22 SPECIAL SESSION: THE PAST, PRESENT, AND FUTURE OF EDA: A CELEBRATION OF 50 YEARS OF DAC

Room: 12AB
General Interest

The 50th Anniversary of the Design Automation Conference is a momentous occasion. Celebrate DAC in this historical session, featuring entertaining and thought-provoking perspectives of the first 25, the second 25, and the next 25 years of Electronic Design Automation.

Chair:
Soha Hassoun - *Tufts Univ., Medford, MA*

22.1 EDA: The First 25 Years (9:00am)
William Joyner - *Semiconductor Research Corporation, Research Triangle Park, NC*

22.2 EDA: The Second 25 Years (9:30am)
Rob Rutenbar - *Univ. of Illinois, Urbana, IL*

22.3 EDA: The Next 25 Years (10:00am)
Leon Stok - *IBM Corp., Hopewell Junction, NY*

23 HUFF AND PUF

Room: 11AB
Embedded System Validation and Verification

First, we build systems for speed and efficiency. Then, we spend a lot of time worrying about how safe and secure they are. Can we change this thought process? What if we built systems that were reliable and secure in the first place? What if we make security and resilience themes in our chip design, instead of time to market? Come think of these and other mind bending ways to design the next generation of chips! With physically unclonable functions, verification mechanisms for ensuring trust in hardware and spatio-temporal error tolerance for processors, this session will tickle your grey cells!

Chair:
Sashi Obilisetty - *Synopsys, Inc., Mountain View, CA*

23.1 A Transmission Gate Physical Unclonable Function and On-Chip Voltage-to-Digital Conversion Technique (9:00am)
Raj Chakraborty, Charles Lamech - *Intel Corp., Hillsboro, OR*
Dhruva Acharyya - *Advantest America, Inc., Cupertino, CA*
Jim Plusquellic - *Univ. of New Mexico, Albuquerque, NM*

23.2 RESP: A Robust Physical Unclonable Function Retrofitted into Embedded SRAM Array (9:15am)
Yu Zheng, Maryam Hashemian, Swarup Bhunia - *Case Western Reserve Univ., Cleveland, OH*

23.3 VeriTrust: Verification for Hardware Trust (9:30am)
Jie Zhang, Feng Yuan, Lingxiao Wei, Zelong Sun, Qiang Xu - *The Chinese Univ. of Hong Kong, , Hong Kong*

23.4 RASTER: Runtime Adaptive Spatial/Temporal Error Resiliency for Embedded Processors (9:45am)
Tuo Li - *Univ. of New South Wales, Sydney, Australia*
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Jude Ambrose - *Univ. of New South Wales, Syndey, Australia*
Semeen Rehman, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

24 SECRETS OF ANALOG VERIFICATION

Room: 13AB
Verification and Simulation

TS

Accurate and efficient analog verification has become a key bottleneck in system-level performance verification. In this session, a diverse group of new algorithms is presented to address the challenges in analog verification. A technique is proposed to produce accurate Boolean models of continuous linear systems, based on which the existing Boolean system verification techniques can be utilized for analog verification. A Bayesian framework is introduced to explore data correlation for efficient performance modeling and verification of analog circuits. A machine learning approach and a hybrid reachability analysis are proposed to verify digitally intensive analog circuits.

Chair:
Trent McConaghy - *Solido Design Automation, Inc., Vancouver, BC, Canada*

24.1 ABCD-L: Approximating Continuous Linear Systems Using Boolean Models (9:00am)
Aadithya Karthik, Jaijeet Roychowdhury - *Univ. of California, Berkeley, CA*

24.2 Bayesian Model Fusion: Large-Scale Performance Modeling of Analog and Mixed-Signal Circuits by Reusing Early-Stage Data (9:15am)
Fa Wang, Wangyang Zhang, Shupeng Sun, Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Chenjie Gu - *Intel Corp., Hillsboro, OR*

24.3 Efficient Moment Estimation with Extremely Small Sample Size via Bayesian Inference for Analog/Mixed-Signal Validation (9:30am)
Chenjie Gu, Eli Chiprout - *Intel Corp., Hillsboro, OR*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

24.4 Verification of Digitally-Intensive Analog Circuits via Kernel Ridge Regression and Hybrid Reachability Analysis (9:45am)
Honghuang Lin, Peng Li - *Texas A&M Univ., College Station, TX*
Chris Myers - *Univ. of Utah, Salt Lake City, UT*

25 LITHO IS HOT!

Room: 14
Design for Manufacturability

This section will show case advances in lithography. Two papers on hot spot detection are presented, one by machine learning and another by fuzzy matching. The approaches have highly accuracy and low false alarm. Then, a novel and efficient method for triple patterning layout decomposition is revealed. Electron beam lithography (EBL) is a promising maskless solution for the technology beyond 14nm logic node. To overcome its throughput limitation, the final paper proposes a tool to solve the overlapping aware stencil planning (OSP) problems in MCC system. In short, this session has all the hot litho topics covered.

Chair:
Fedor Pikus - *Mentor Graphics Corp., Wilsonville, OR*

25.1 Machine-Learning-Based Hotspot Detection Using Topological Classification and Critical Feature Extraction (9:00am)
Yen-Ting Yu, Geng-He Lin, Iris Hui-Ru Jiang - *National Chiao Tung Univ., Hsinchu, Taiwan*
Charles Chiang - *Synopsys, Inc., Mountain View, CA*

25.2 A Novel Fuzzy Matching Model for Lithography Hotspot Detection (9:15am)
Sheng-Yuan Lin, **Jing-Yi Chen**, Jin-Cheng Li, Wan-Yu Wen, Shih-Chieh Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*

25.3 An Efficient Layout Decomposition Approach for Triple Patterning Lithography (9:30am)
Jian Kuang, Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong, , Hong Kong*

25.4 E-BLOW: E-Beam Lithography Overlapping Aware Stencil Planning for MCC System (9:45am)
Bei Yu - *Univ. of Texas at Austin, TX*
Kun Yuan - *Cadence Design Systems, Inc., Austin, TX*
Jhih-Rong Gao, David Pan - *Univ. of Texas at Austin, TX*

26 UNDERSTANDING MOTHER NATURE AND TAMING ITS WRATH

Room: 15
Test and Reliability

Alleviating the impact of uncertainties in the semiconductor fabrication process necessitates methods for modeling process variations and dealing with defects. This session elucidates the impact of process variations on die and wafer populations and introduces solutions for testing and repairing 3D ICs.

Chair:
Ken Butler - *Texas Instruments, Inc., Dallas, TX*

26.1 Automatic Clustering of Wafer Spatial Signatures (9:00am)
Wangyang Zhang, Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Sharad Saxena - *PDF Solutions, Richardson, TX*
Andrzej Strojwas - *Carnegie Mellon Univ., Pittsburgh, PA*
Rob Rutenbar - *Univ. of Illinois, Urbana, IL*

26.2 Multidimensional Analog Test Metrics Estimation Using Extreme Value Theory and Statistical Blockade (9:15am)
Haralampos-G. Stratigopoulos - *TIMA Laboratory, CNRS/Grenoble INP/UJF, Grenoble, France*
Pierre Faubet, Yoann Courant, Firas Mohamed - *Infiniscale SA, Grenoble, France*

26.3 High-Throughput TSV Testing and Characterization for 3D Integration Using Thermal Mapping (9:30am)
Kapil Dev - *Brown Univ., Providence, RI*
Gary Woods - *Rice Univ., Houston, TX*
Sherief Reda - *Brown Univ., Providence, RI*

26.4 On Effective and Efficient In-Field TSV Repair for Stacked 3D ICs (9:45am)
Li Jiang, Qiang Xu - *The Chinese Univ. of Hong Kong, , Hong Kong*
Fangming Ye, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Bill Eklow - *Cisco Systems, Inc., San Jose, CA*

27 PANEL: TEST/DIAGNOSE/DEBUG: LET THE 3D-IC CHAOS BEGIN

Room: 16AB
Test and Reliability

TS

2.5D and 3D chips are moving from the lab and into production. The first data are coming from the field. There are many open questions on how to get adequate testing through the manufacturing and assembly process to ensure the economic viability of the 3D-IC. This panel will debate which are the most critical open issues related to the test, diagnosis and debug processes and suggest solutions and metrics.

Moderator:
Bill Eklow - *Cisco Systems, Inc., San Jose, CA*

Panelists:
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Al Crouch - *ASSET InterTech, Inc., Cedar Park, TX*
Mike Shapiro - *IBM Corp., Austin, TX*
Shahin Toutounchi - *Xilinx, Inc., San Jose, CA*

SESSION 33: SKY TALK: 2:30 - 3:00PM
21st Century Digital Design Tools

28 SPECIAL SESSION: THE FUTURE OF OPERATING SYSTEMS FOR EMBEDDED SYSTEMS AND SOFTWARE (ESS)

Room: 12AB
Embedded Software

This session aims at providing a first attempt in the direction of presenting advances in operating system research targeting Embedded Systems and Software (ESS). Researchers from both industries and universities who are working on novel ESS computing systems and focusing their attention and effort at the OS level are invited to present their recent contributions and future directions. We will have the chance to have contributions investigating cutting-edge solutions which incorporate new advances in conventional OS services for embedded systems such as scheduling and resources management while including novel research prospective in OS design for ESS such as dynamically adaptable OS, self-aware OS services and distributed factored OS research.

Chair:
Simone Campanoni - *Harvard Univ., Cambridge, MA*

28.1 Cloud Platforms and Embedded Computing -- The Operating Systems of the Future (1:30pm)
Jan Rellermeyer - *IBM Research - Austin, TX*
Seong-Won Lee - *Seoul National Univ., IBM Research - Austin, Seoul, Republic of Korea*
Michael Kistler - *IBM Research - Austin, TX*

28.2 Tessellation: Refactoring the OS around Explicit Resource Containers with Continuous Adaptation (2:00pm)
John Kubiatowicz - *Univ. of California, Berkeley, CA*
Juan Colmenares - *Samsung, San Jose, CA*
Greg Eads - *Univ. of California, Berkeley, CA*
Steven Hofmeyr - *Lawrence Berkeley National Lab, Berkeley, CA*
Sarah Bird, Miguel Moreto, David Chou - *Univ. of California, Berkeley, CA*
Brian Gluzman - *Univ. of California, Davis, CA*
Eric Roman - *Lawrence Berkeley National Lab, Berkeley, CA*
Davide Bartolini, Nitesh Mor, Krste Asanovic - *Univ. of California, Berkeley, CA*

28.3 The Autonomic Operating System Research Project - Achievements and Future Directions (2:30pm)
Davide Bartolini, Riccardo Cattaneo, Gianluca Durelli - *Politecnico di Milano, Milan, Italy*
Martina Maggio - *Lund Univ., Lund, Sweden*
Marco Santambrogio, Filippo Sironi - *Politecnico di Milano, Milan, Italy*

29 CAPTCHA THE CHIP!

Room: 11AB
Embedded System Validation and Verification

Trust has become an important design concern spanning software and hardware in embedded systems. Outsourcing of design, fabrication and test steps enables a variety of attacks on ICs. This session highlights practical attacks based on analyzing power dissipation and injecting malware to capture a chip. It presents defenses at the power grid, processor architecture and compiled code levels.

Chair:
Jim Plusquellic - *Univ. of New Mexico, Albuquerque, NM*

29.1 Role of Power Grid in Side Channel Attack and Power-Grid-Aware Secure Design (1:30pm)
Xinmu Wang - *Case Western Reserve Univ., Cleveland, OH*
Wen Yueh, Saibal Mukhopadhyay - *Georgia Institute of Technology, Atlanta, GA*
Debapriya Basu Roy, Debdeep Mukhopadhyay - *Indian Institute of Technology, Kharagpur, India*
Seetharam Narasimhan - *Intel Corp., Cleveland, OH*
Yu Zheng, **Swarup Bhunia** - *Case Western Reserve Univ., Cleveland, OH*

29.2 NumChecker: Detecting Kernel Control-Flow Modifying Rootkits by Using Hardware Performance Counters (1:45pm)
Xueyang Wang, Ramesh Karri - *Polytechnic Institute of New York Univ., Brooklyn, NY*

29.3 High-Performance Hardware Monitors to Protect Network Processors from Data Plane Attacks (2:00pm)
Harikrishnan Chandrikakutty, Deepak Unnikrishnan - *Univ. of Massachusetts, Amherst, MA*
Russell Tessier - *Univ. of Massachusetts, Amherst, MA*
Tilman Wolf - *Univ. of Massachusetts, Amherst, MA*

29.4 Compiler-Based Side Channel Vulnerability Analysis and Optimized Countermeasures Application (2:15pm)
Giovanni Agosta, Alessandro Barenghi, Massimo Maggi, **Gerardo Pelosi** - *Politecnico di Milano, Milan, Italy*

TS

30 MULTI CHALLENGES OF EMBEDDED MULTI-PROCESSING

Room: 13AB
Embedded Architecture & Platforms

Heterogeneity shows up from device to high-level processor architecture. Significant challenges emerge in maintaining coherence in multiprocessor SoCs, virtualization, and cache reliability. This session addresses these challenging directions by making critical observations, presenting novel solutions, and comprehensive experimental evaluation.

Chair:
Mohammad Al Faruque - *Univ. of California, Irvine, CA*

30.1 Lighting the Dark Silicon by Exploiting Heterogeneity on Future Processors (1:30pm)
Ying Zhang, Lu Peng - *Louisiana State Univ., Baton Rouge, LA*
Xin Fu - *Univ. of Kansas, Lawrence, KS*
Yue Hu - *Louisiana State Univ., Baton Rouge, LA*

30.2 Simultaneous Multithreading Support in Embedded Distributed Memory MPSoCs (1:45pm)
Rafael Garibotti - *Univ. Montpellier 2, Montpellier, France*
Luciano Ost - *Laboratoire d'Informatique de Grenoble, Montpellier, France*
Remi Busseuil, Mamady Kourouma - *Univ. Montpellier 2, Montpellier, France*
Chris Adeniyi-Jones - *ARM, Ltd., Cambridge, United Kingdom*
Gilles Sassatelli, Michel Robert - *Univ. Montpellier 2, Montpellier, France*

30.3 APPLE: Adaptive Performance-Predictable Low-Energy Caches for Reliable Hybrid Voltage Operation (2:00pm)
Bojan Maric, Jaume Abella, Mateo Valero - *Barcelona Supercomputing Ctr., Barcelona, Spain*

30.4 An Optimized Page Translation for Mobile Virtualization (2:15pm)
Yuan-Cheng Lee, Chih-Wen Hsueh - *National Taiwan Univ., Taipei, Taiwan*

31 ACCELERATED SIMULATION AND VERIFICATION FOR POWER GRID AND MEMORY

Room: 14
Verification and Simulation

Power delivery networks are crucial components of modern digital design. Their simulation and verification pose big challenges. Vector-less verification techniques are promising approaches to analyze large-scale power grids without explicit simulation. Large current densities make verification of electromigration in power grid a unique and difficult task. The final paper presents an efficient implementation of SPICE simulation on GPU architectures.

Chair:
Florentin Dartu - *Synopsys, Inc., Hillsboro, OR*

31.1 Scalable Vectorless Power Grid Current Integrity Verification (1:30pm)
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

31.2 Constraint Abstraction for Vectorless Power Grid Verification (1:45pm)
Xuanxing Xiong, Jia Wang - *Illinois Institute of Technology, Chicago, IL*

31.3 The Impact of Electromigration in Copper Interconnects on Power Grid Integrity (2:00pm)
Vivek Mishra, Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

31.4 TinySPICE: A Parallel SPICE Simulator on GPU for Massively Repeated Small Circuit Simulations (2:15pm)
Lengfei Han, Xueqian Zhao, Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

32 WE'RE GONNA ROUTE AROUND THE CLOCK

Room: 15
Physical Design

Design sizes are exploding. The complexity of the wire stack is increasing. Design rules are numbingly complex. The importance of routing and clock network synthesis in this environment has never been more critical. But never fear, there's a party going on right here. This session addresses issues in clock skew variation, clock power, routing congestion estimation for real world designs, and spacer-is-dielectric-compliant detailed routing. Come route around the clock with us!

Chair:
Mehmet Yildiz - *Synopsys, Inc., Austin, TX*

32.1 An Optimal Algorithm of Adjustable Delay Buffer Insertion for Solving Clock Skew Variation Problem (1:30pm)
Juyeon Kim, Deokjin Joo, Taewhan Kim - *Seoul National Univ., Seoul, Republic of Korea*

32.2 Smart Non-Default Routing for Clock Power Reduction (1:45pm)
Andrew B. Kahng, Seokhyeong Kang, **Hyein Lee** - *Univ. of California at San Diego, La Jolla, CA*

32.3 Routing Congestion Estimation with Real Design Constraints (2:00pm)
Wen-Hao Liu - *National Chiao Tung Univ., Hsinchu, Taiwan*
Yaoguang Wei, Cliff Sze, Charles Alpert, Zhuo Li - *IBM Research - Austin, TX*
Yih-Lang Li - *National Chiao Tung Univ., Hsin-Chu, Taiwan*
Natarajan Viswanathan - *IBM Systems and Technology Group, Austin, TX*

32.4 Spacer-Is-Dielectric-Compliant Detailed Routing for Self-Aligned Double Patterning Lithography (2:15pm)
Yuelin Du, Martin D. F. Wong - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Qiang Ma, Hua Song, James Shiely, Gerard Luk-Pat, Alexander Miloslavsky - *Synopsys, Inc., Mountain View, CA*

34 PANEL: EDA: MEET ANALYTICS; ANALYTICS: MEET EDA

Room: 16AB
Emerging Design Technologies

TS

The sheer scale of data generated by EDA tools used on an system-on-chip (SoC) suggest that analytics should play a major role in speedy SoC completion. This is especially true for Functional Verification where analytics can be helpful in sizing the problem, assessing progress, and improving process. However, beyond familiar coverage metrics, this is not the case today. This panel considers statistical analysis, data mining, machine learning, and other analytic methods to gain more insight into verification – and whether the analytics approach can extend to other SoC design areas.

Moderator:
Janick Bergeron - *Synopsys, Inc., Ottawa, ON, Canada*

Panelists:
Jay Bhadra - *Freescale Semiconductor, Inc., Austin, TX*
Harry Foster - *Mentor Graphics Corp., Plano, TX*
Li-C Wang - *Univ. of California, Santa Barbara, CA*
Avi Ziv - *IBM Haifa Research Lab., Haifa, Israel*
Fei Xie - *Portland State Univ., Portland, OR*

SESSION 40: SKY TALK: 5:30 - 6:00PM
The Role of Cascade, a Cycle-Based Simulation Infrastructure, in Designing the Anton Special-Purpose Supercomputers

35 SPECIAL SESSION: ELECTRONICS AND SOFTWARE ON WHEELS: EMBEDDED SYSTEMS DESIGN CHALLENGES FOR ELECTRIC VEHICLES AND THE PATH AHEAD

Room: 12AB
Embedded Design Methodologies

Electromobility poses an important challenge for the academia and the industry both in Europe as well as in North America. Modern high-end cars today have as many as 100 ECUs and run more than 100 million lines of code. The architecture and software design for electric vehicles will however need a substantial redesign and pose a number of embedded systems and software challenges. These include ECU consolidation, virtualization, increased need for virtual integration and model-based hw/sw development, predictable time-triggered architectures, the use of hybrid batteries and their management, and increased hardware and software reliability. Further more problems related to security, verification and certification will also need to be solved. This session will feature a number of talks that will discuss these challenges, the current state-of-the-art especially in terms of practices and tools being used in the industry and discuss what lies ahead in this area. Electric Vehicles pose unique architecture and software design challenges that need considerable engagement from embedded systems researchers and practitioners in the near future.

Chair:
Andreas Herkersdorf - *Technical Univ. of Munich, Munich, Germany*

35.1 System Architecture and Software Design for Electric Vehicles (4:00pm)
Martin Lukasiewycz, Sebastian Steinhorst, Sidharta Andalam, Florian Sagstetter, Peter Waszecki, Wanli Chang, Matthias Kauer, Philipp Mundhenk - *TUM CREATE Ltd., Singapore*
Shreejith Shanker, Suhaib Fahmy - *Nanyang Technological Univ., Singapore*
Samarjit Chakraborty - *Technical Univ. of Munich, Munich, Germany*

35.2 Model-Based Software Development, Verification, and Certification for Electric Vehicles (4:30pm)
Dip Goswami - *Technical Univ. of Munich, Munich, Germany*
Martin Lukasiewycz, Matthias Kauer, Sebastian Steinhorst - *TUM CREATE Ltd., Singapore*
Alejandro Masrur, Samarjit Chakraborty - *Technical Univ. of Munich, Munich, Germany*
S. Ramesh - *General Motors Company, Warren, MI*

35.3 Hybrid Energy Storage Systems and Battery Management for Electric Vehicles (5:00pm)
Naehyuck Chang, Sangyoung Park, Younghyun Kim - *Seoul National Univ., Seoul, Republic of Korea*

35.4 Coping with Security Challenges in EVs: Implications on Architecture and Software Design (5:30pm)
Andre Weimerskirch - *ESCRYPT Inc., Ann Arbor, MI*

35.5 Reliability Challenges for Electric Vehicles: From Devices to Architecture and Systems Software (6:00pm)
Georg Georgakos - *Infineon Technologies AG, Munich, Germany*
Ulf Schlichtmann, Reinhard Schneider, Samarjit Chakraborty - *Technical Univ. of Munich, Munich, Germany*

36 ADVENTURES IN TIME AND SPACE: TARGETING RESILIENCY

Room: 11AB
Test and Reliability

TS

Embark on a trip to the land of reliability and explore how current and future techniques will save us all from decaying and unpredictable chips. Gain a new "perspective" on the state-of-the-art and upcoming trends in reliable design and modeling through a survey of error sources and solutions. Discover new insights on transient error analysis and protection techniques in the context of memories, microprocessors, and general logic circuits.

Chair:
Al Crouch - *ASSET InterTech, Inc., Cedar Park, TX*

36.1 Reliable On-Chip Systems in the Nano-Era: Lessons Learnt and Future Trends (4:00pm)
Jörg Henkel, Lars Bauer - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Nikil Dutt - *Univ. of California, Irvine, CA*
Puneet Gupta - *Univ. of California, Los Angeles, CA*
Sani Nassif - *IBM Research, Austin, TX*
Muhammad Shafique, Mehdi Tahoori - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Norbert Wehn - *Technische Univ. Kaiserslautern, Kaiserslautern, Germany*

36.2 A Layout-Based Approach for Multiple Event Transient Analysis (4:30pm)
Mojtaba Ebrahimi - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Hossein Asadi - *Sharif Univ. of Technology, Tehran, Iran*
Mehdi Tahoori - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

36.3 Quantitative Evaluation of Soft Error Injection Techniques for Robust System Design (4:45pm)
Hyungmin Cho - *Stanford Univ., Stanford, CA*
Shahrzad Mirkhani - *Univ. of Texas at Austin, TX*
Chen-Yong Cher - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Jacob Abraham - *Univ. of Texas at Austin, TX*
Subhasish Mitra - *Stanford Univ., Stanford, CA*

36.4 Efficiently Tolerating Timing Violations in Pipelined Microprocessors (5:00pm)
Koushik Chakraborty, Brennan Cozzens, Sanghamitra Roy, Dean Ancajas - *Utah State Univ., Logan, UT*

36.5 Hierarchical Decoding of Double Error Correcting Codes for High Speed Reliable Memories (5:15pm)
Zhen Wang - *MediaTek, Inc., Woburn, MA*

37 NEW FRONTIERS IN EDA: FROM BEYOND CMOS TO MORE THAN MOORE

Room: 13AB
Emerging Design Technologies

In this session, you will be introduced to a wide range of disruptive technologies spanning the digital, analog, and memory application spaces. Beginning with an introduction to transistor-level monothilic 3D integration, it transitions to novel logic technologies based on carbon nanotubes and nano-magnets. Optimization and neuromorphic applications of non-volatile memories and tunneling transistors for low power analog electronics round off this exciting tour of the computing landscape of the future.

Chair:
Syed Alam - *Everspin Technologies, Inc., Mountain View, CA*

37.1 Power Benefit Study for Ultra-High Density Transistor-Level Monolithic 3D ICs (4:00pm)
Young-Joon Lee, Daniel Limbrick, **Sung Kyu Lim** - *Georgia Institute of Technology, Atlanta, GA*

37.2 Rapid Exploration of Processing and Design Guidelines to Overcome Carbon Nanotube Variations (4:15pm)
Gage Hills - *Stanford Univ., Stanford, CA*
Jie Zhang - *Google, Inc., Mountain View, CA*
Charles Mackin - *Massachusetts Institute of Technology, Cambridge, MA*
Max Shulaker, Hai Wei, H.S. Philip Wong, Subhasish Mitra - *Stanford Univ., Stanford, CA*

37.3 Minimum-Energy State Guided Physical Design for Nanomagnet Logic(4:30pm)
Shiliang Liu, Gyorgy Csaba, Xiaobo Sharon Hu, Edit Varga, Michael Niemier, Gary Bernstein, Wolfgang Porod - *Univ. of Notre Dame, Notre Dame, IN*

37.4 Ultra Low Power Associative Computing with Spin Neurons and Resistive Crossbar Memory (4:45pm)
Mrigank Sharad, Deliang Fan, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

37.5 Understanding the Trade-Offs in Multi-Level Cell ReRAM Memory Design (5:00pm)
Cong Xu, Dimin Niu - *Pennsylvania State Univ., University Park, PA*
Naveen Muralimanohar - *Hewlett-Packard Labs., Santa Clara, CA*
Norman Jouppi - *Hewlett-Packard Co., Palo Alto, CA*
Yuan Xie - *Pennsylvania State Univ., Advanced Micro Devices, Inc., University Park, PA*

37.6 Exploring Tunnel-FET for Ultra Low Power Analog Applications: A Case Study on Operational Transconductance Amplifier (5:15pm)
Amit Trivedi, Sergio Carlo, Saibal Mukhopadhyay - *Georgia Institute of Technology, Atlanta, GA*

38 NOVEL APPLICATION SCENARIOS FOR DVFS TECHNIQUES

Room: 14
Low-Power Design and Power Analysis

TS

Dynamic Voltage and Frequency Scaling (DVFS) techniques have traditionally been proposed as efficient mechanisms for power optimization in multi-processor systems. However, they open new issues regarding implementation constraints and emerging application scenarios. This session addresses the novel application scenarios that appear nowadays when DVFS techniques are applied. The first three papers address different issues related to the tradeoff between energy and error probability. The fourth paper proposes a new methodology to quantify application resilience. The final two papers explore new applications of DVFS in multicores, shared components and multimedia applications.

Chair:
Qinru Qiu - *Syracuse Univ., Syracuse, NY*

38.1 Energy-Optimal SRAM Supply Voltage Scheduling under Lifetime and Error Constraints (4:00pm)
Andrea Calimera, **Massimo Poncino**, Enrico Macii - *Politecnico di Torino, Torino, Italy*

38.2 Relax-and-Retime: A methodology for Energy-Efficient Recovery based Design (4:15pm)
Shankar Ganesh Ramasubramanian, Swagath Venkataramani, Adithya Parandhaman, Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

38.3 Post-Placement Voltage Island Generation for Timing-Speculative Circuits (4:30pm)
Rong Ye, Feng Yuan, Zelong Sun - *The Chinese Univ. of Hong Kong, Hong Kong*
Wen-Ben Jone - *Univ. of Cincinnati, Cincinnati, OH*
Qiang Xu - *The Chinese Univ. of Hong Kong, , Hong Kong*

38.4 Analysis and Characterization of Inherent Application Resilience for Approximate Computing (4:45pm)
Vinay Chippa - *Purdue Univ., West Lafayette, IN*
Srimat Chakradhar - *NEC Labs America, Inc., Princeton, NJ*
Kaushik Roy, Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

38.5 Dynamic Voltage and Frequency Scaling for Shared Resources in Multicore Processor Designs (5:00pm)
Xi Chen, Zheng Xu, Hyungjun Kim, **Paul Gratz**, Jiang Hu - *Texas A&M Univ., College Station, TX*
Michael Kishinevsky, Umit Ogras, Raid Ayoub - *Intel Corp., Hillsboro, OR*

38.6 Energy Optimization by Exploiting Execution Slacks in Streaming Applications on Multiprocessor Systems (5:15pm)
Amit Kumar Singh, Anup Das, Akash Kumar - *National Univ. of Singapore, Singapore*

39 VERIFICATION: FROM SYSTEMC TO THE REALITY OF SILICON

Room: 15
Verification and Simulation

The verification bottleneck is becoming increasingly acute as design complexity balloons and time-to-market shrinks. Meeting the challenge requires creative use of both formal and simulation-based techniques at all stages of design, from high-level behavioral models to final implementation and at scales from the block up to the system level. The papers in this session address symbolic simulation of SystemC designs, equivalence checking for behavioral synthesis, both formal and constrained random techniques for RTL design verification, and the application of post-silicon constrained random verification.

Chair:
Jason Baumgartner - *IBM Systems and Technology Group, Austin, TX*

39.1 Verifying SystemC using an Intermediate Verification Language and Symbolic Simulation (4:00pm)
Hoang Le, Daniel Grosse, Vladimir Herdt, Rolf Drechsler - *Univ. of Bremen, Bremen, Germany*

39.2 Handling Design and Implementation Optimizations in Equivalence Checking for Behavioral Synthesis (4:15pm)
Zhenkun Yang, Kecheng Hao - *Portland State Univ., San Jose, CA*
Sandip Ray - *Univ. of Texas at Austin, TX*
Fei Xie - *Portland State Univ., Portland, OR*

39.3 A Counterexample-Guided Interpolant Generation Algorithm for SAT-based Model Checking (4:30pm)
Cheng-Yin Wu, Chi-An Wu, Chien-Yu Lai, Chung-Yang (Ric) Huang - *National Taiwan Univ., Taipei, Taiwan*

39.4 A Robust Constraint Solving Framework for Multiple Constraint Sets in Constrained Random Verification (4:45pm)
Bo-Han Wu, Chung-Yang (Ric) Huang - *National Taiwan Univ., Taipei, Taiwan*

39.5 Simulation Knowledge Extraction and Reuse in Constrained Random Processor Verification (5:00pm)
Wen Chen, Li-Chung Wang - *Univ. of California, Santa Barbara, CA*
Jay Bhadra, Magdy Abadir - *Freescale Semiconductor, Inc., Austin, TX*

39.6 Hardware-Efficient On-Chip Generation of Time-Extensive Constrained-Random Sequences for In-System Validation (5:15pm)
Adam Kinsman, **Ho Fai Ko**, Nicola Nicolici - *McMaster Univ., Hamilton, ON, Canada*

41 PANEL: BARRIERS TO THE INTERNET OF THINGS: EMBEDDED SOFTWARE, SECURITY, COST, POWER?

Room: 16AB
System Level Design and Communication

TS

The Internet of Things is being hyped as the next big thing. All kinds of everyday products will have intelligence and a network connection will be controlled by mobile devices and will send data to the cloud. For example, your toaster or your glasses can talk to the cloud. That all sounds great, but what will be the barriers to growth: embedded software, security, cost or power? Or, is it the unstoppable next wave?

Moderator:
Richard House - *Cisco Systems, Inc., Austin, TX*

Panelists:
Brian Gildon - *Timesys Corp., Austin, TX*
John Heinlein - *ARM, Inc., San Jose, CA*
Edward Lee - *Univ. of California, Berkeley, CA*
Geng Lin - *Dell Inc., San Jose, CA*
Diwakar Vishakhadatta - *Silicon Laboratories, Inc., Austin, TX*

42 SPECIAL SESSION: THE FUTURE IS HERE: LIVE DEMOS OF THE "NEXT" TRANSISTOR

Room: 12AB
Emerging Design Technologies

Novel and emerging technologies will push Moore's Law beyond the traditional CMOS limits. Recently, research groups demonstrated maturity that goes beyond the device community and enabled the design of complex circuits. The session will show through live demos that design can efficiently take advantages of the novel properties brought by the next generation devices. The talks will cover a broad range of technologies (Si Nanowires, Carbon Nanotubes, Organic electronics, Spintronic, Advanced CMOS) and applications (ASICs, FPGAs, Sensors).

Chair:
Fabien Clermidy - *CEA-LETI, Grenoble, France*

42.1 Towards Structured ASICs Using Polarity Tunable Si Nanowire Transistors (9:00am)
Pierre-Emmanuel Gaillardon, Michele De Marchi, Luca Amarù, Shashikanth Bobba, Davide Sacchetto, Yusuf Leblebici, Giovanni De Micheli - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*

42.2 Sacha: The Stanford Carbon Nanotube Controlled Handshaking Robot (9:30am)
Max Shulaker - *Stanford Univ., Stanford, CA*
Jelle Van Rethy - *Katholieke Univ. Leuven, Belgium*
Gage Hills, Hong-Yu Chen - *Stanford Univ., Stanford, CA*
Georges Gielen - *Katholieke Univ. Leuven, Belgium*
H.-S. Philip Wong, Subhasish Mitra - *Stanford Univ., Stanford, CA*

42.3 Electrical Artificial Skin Using Ultra-Flexible Organic Transistor (10:00am)
Tsuyoshi Sekitani, Tomoyuki Yokota, Makoto Takamiya, Takayasu Sakurai, Takao Someya - *Univ. of Tokyo, Tokyo, Japan*

42.4 Non-Volatile FPGAs Based on Spintronic Devices (10:30am)
Guillaume Prenat, Olivier Goncalves, Gregory Di Pendina, Bernard Dieny - *Spintec, CEA-INAC/CNRS/UJF/INPG, Grenoble, France*

42.5 Relays do not Leak – CMOS Does (11:00am)
Hossein Fariborzi - *Massachusetts Institute of Technology, Cambridge, MA*
Fred Chen - *OnChip Power Corp., Boston, MA*
Rhesa Nathanael, I-Ru Chen, Louis Hutin - *Univ. of California, Berkeley, CA*
Rinus Lee - *SEMATECH, Albany, NY*
Vladimir Stojanovic - *Massachusetts Institute of Technology, Cambridge, MA*
Tsu-Jae King Liu - *Univ. of California, Berkeley, CA*

42.6 Single-Photon Image Sensors (11:30am)
Edoardo Charbon, Francesco Regazzoni - *Delft Univ. of Technology, Delft, The Netherlands*

43 SYSTEM COMPILATION FOR MULTI-CORES: ANALYSIS AND SYNTHESIS

Room: 11AB
System Level Design and Communication

Complexity and heterogeneity of multi-core applications and architectures is increasing at an unprecedented pace. This demands system compilers that can automatically and optimally map dynamic applications onto parallel and distributed on-chip architectures. This session covers aspects of the system compilation process ranging from static timing analysis over run-time task mapping optimizations to joint system-level and micro-architecture exploration.

Chair:
Christian Haubelt - *Univ. of Rostock, Rostock, Denmark*

43.1 A Novel Analytical Method for Worst Case Response Time Estimation of Distributed Embedded Systems (9:00am)
Jinwoo Kim - *Seoul National Univ., Seoul, Republic of Korea*
Hyunok Oh - *Hanyang Univ., Seoul, Republic of Korea*
Junchul Choi, Hyojin Ha, Soonhoi Ha - *Seoul National Univ., Seoul, Republic of Korea*

43.2 Optimizations for Configuring and Mapping Software Pipelines in Many Core Systems (9:15am)
Janmartin Jahn, Santiago Pagani, Sebastian Kobbe, Jian-Jia Chen, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

43.3 A Scenario-Based Run-Time Task Mapping Algorithm for MPSoCs (9:30am)
Wei Quan, Andy Pimentel - *Univ. of Amsterdam, Amsterdam, The Netherlands*

43.4 Early Exploration for Platform Architecture Instantiation with Multi-Mode Application Partitioning (9:45am)
Prashant Agrawal, Praveen Raghavan, Matthias Hartmann - *IMEC, Heverlee, Belgium*
Namita Sharma - *Indian Institute of Technology, New Delhi, India*
Liesbet Van der Perre, Francky Catthoor - *IMEC, Leuven, Belgium*

44 EMBEDDED: WHEN APPLICATIONS AND ARCHITECTURES COLLIDE

Room: 13AB
Embedded Architecture & Platforms

TS

Recent progress in embedded systems has enabled innovative applications. Challenges that must be overcome include application-specific requirements and severe constraints on power, area, and performance. This session showcases excellent designs that advance the state-of-the-art in cryptography, wireless communication, biologically-inspired recognition systems, and ultra low power image processing.

Chair:
Walid Najjar - *Univ. of California, Riverside, CA*

44.1 CoARX: A Coprocessor for ARX-Based Cryptographic Algorithms (9:00am)
Khawar Shahzad, Ayesha Khalid, Zoltán Rákossy - *RWTH Aachen Univ., Aachen, Germany*
Goutam Paul - *Jadavpur Univ., Kolkata, India*
Anupam Chattopadhyay - *RWTH Aachen Univ., Aachen, Germany*

44.2 Reconfigurable Pipelined Coprocessor for Multi-Mode Communication Transmission (9:15am)
Liang Tang, Jude Ambrose, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

44.3 Accelerators for Biologically-Inspired Attention and Recognition (9:30am)
Mi Sun Park - *Pennsylvania State Univ., University Park, PA*
Chuanjun Zhang - *Intel Corp., Pittsburgh, PA*
Michael DeBole - *IBM Corp., Poughkeepsie, NY*
Srinidhi Kestur, Vijaykrishnan Narayanan, Mary Jane Irwin - *Pennsylvania State Univ., University Park, PA*

44.4 Stochastic Circuits for Real-Time Image-Processing Applications (9:45am)
Armin Alaghi, Cheng Li, John Hayes - *Univ. of Michigan, Ann Arbor, MI*

45 SPECIAL SESSION: 3D-IC DESIGN: WHERE ARE WE GOING FROM HERE?

Room: 14
Emerging Design Technologies

In the last several years, a lot of progress has been made in 3D integration from system-level design to fabrication technology. However, 3D-IC products are not making the large stride into the semiconductor market as expected. The reasons behind this may due to many factors including both technical and nontechnical challenges.

This session invites experts from both industry and academia to reflect on the most recent advancement in 3D integration, where 3D integration is heading, and what road blocks need to be removed along the way. The discussions will make specific connection to the design, tool, fabrication and test issues related to 3D-IC technology.

Chair:
Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*

45.1 Where are all Those 3D Chips? (9:00am)
Robert Patti - *Tezzaron Semiconductor, Naperville, IL*

45.2 The Industry's First 3D FPGA (9:30am)
Ephrem Wu - *Xilinx, Inc., San Jose, CA*

45.3 3D - Waiting for Cost Learning to Occur? (10:00am)
Paul Franzon - *North Carolina State Univ., Raleigh, NC*

46 SPICE UP THE ANALYSIS!!

Room: 15
Circuit and interconnect analysis

Increasing design complexity makes analog mixed signal analysis a major challenge constantly in need of improvement. The papers in this session all target this lofty goal but from different perspectives. Speedier analysis can be achieved through increased abstraction coupled with faster simulation algorithms, improvements in timestep selection, faster extraction or the usage of parallel environments. This session explores some of these facets to beef up analysis efficiency hoping to provide designers with accurate feedback faster.

Chair:
Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology, Abu Dhaibi, United Arab Emirates*

46.1 An Event-Driven Simulation Methodology for Integrated Switching Power Supplies in SystemVerilog (9:00am)
Ji Eun Jang, Myeongjae Park, Jaeha Kim - *Seoul National Univ., Seoul, Republic of Korea*

46.2 A New Time-Stepping Method for Circuit Simulation (9:15am)
G. Peter Fang - *Texas Instruments, Inc., Dallas, TX*

46.3 Time-Domain Segmentation Based Massively Parallel Simulation for ADCs (9:30am)
Zuochang Ye, Bichen Wu - *Tsinghua Univ., Beijing, China*
Song Han - *Stanford Univ., Palo Alto, CA*
Yang Li - *Univ. of Texas at Austin, TX*

46.4 A Direct Finite Element Solver of Linear Complexity for Large-Scale 3D Circuit Extraction in Multiple Dielectrics (9:45am)
Bangda Zhou, Haixin Liu, Dan Jiao - *Purdue Univ., West Lafayette, IN*

47 PANEL: ANALOG DESIGN WITH FINFETS: "THE GODS MUST BE CRAZY!"

Room: 16AB
Analog/Mixed-Signal/RF Design

TS

FinFET devices have emerged as the winner for process nodes beyond 20nm. The advantages are too compelling to ignore. However what's great for SoC is a real challenge for analog. With sub-threshold currents near zero and virtually no bias control capability, suddenly the analog designer will have to throw out the old schematics and really start to rethink the problem. The big question: How quickly will mainstream analog design find its way into FinFET-driven logic processes?

Moderator:
Ron Wilson - *Altera Corp., San Jose, CA*

Panelists:
Anirudh Devgan - *Cadence Design Systems, Inc., Austin, TX*
Scott Herrin - *Freescale Semiconductor, Inc., Austin, TX*
Navraj Nandra - *Synopsys, Inc., Mountain View, CA*
Eric Soenen - *Taiwan Semiconductor Manufacturing Co., Ltd., Austin, TX*

SESSION 53: SKY TALK: 2:30 - 3:00PM
Solving Analog Challenges to Enable the Future of Electronics

48 SPECIAL SESSION: FPGAS AS GENERAL-PURPOSE PROCESSORS: PROGRESS AND CHALLENGES

Room: 12AB
Embedded Architecture & Platforms

Just like GPUs have made the transition from single-purpose devices to more general-purpose programmable processors, the drive towards ever increasing efficiency and performance is making the industry consider FPGAs as more general-purpose compute elements. This session discusses the implications for the design of FPGAs and systems that contain them, and the tool chains required to make these systems usable, ranging from higher-level approaches to programming FPGAs, to new demands on synthesis and mapping.

Chair:
H. Peter Hofstee - *IBM Research - Austin, TX*

48.1 The Role of FPGAs in Heterogeneous Computing and Silicon Convergence (1:30pm)
Misha Burich - *Altera Corp., San Jose, CA*

48.2 FPGA Code Accelerators - The Compiler Perspective (2:00pm)
Walid Najjar - *Univ. of California, Riverside, CA*
Jason Villarreal - *Jacquard Computing Inc., Riverside, CA*

48.3 Innovations in Reconfigurable, Application-Specific Systems (2:30pm)
Steve Wallach - *Convey Computer Corp., Richardson, TX*

49 KEEPING AUSTIN WEIRD DAC-STYLE: WILDER AND CRAZIER IDEAS

Room: 11AB
WACI

Stop wasting your time on pointless research and come hear about what really matters: curing cancer while driving a Mustang filled with Greek warriors, blasting at a petabit per second. Science fiction? No, just the WAClest papers yet.

Chair:
Jacob Abraham - *Univ. of Texas at Austin, TX*

49.1 Can CAD Cure Cancer? (1:30pm)
Smita Krishnaswamy - *Columbia Univ., New York, NY*
Bernd Bodenmiller - *Univ. Zürich, Zurich, Switzerland*
Dana Pe'er - *Columbia Univ., New York, NY*

49.2 Let's put the Car in your Phone! (1:45pm)
Martin Geier, Martin Becker, Daniel Yunge, Benedikt Dietrich, Reinhard Schneider, Dip Goswami, Samarjit Chakraborty - *Technical Univ. of Munich, Munich, Germany*

49.3 The Undetectable and Unprovable Hardware Trojan Horse (2:00pm)
Sheng Wei, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

49.4 Path to a TeraByte of On-Chip Memory for Petabit per Second Bandwidth with < 5Watts of Power (2:15pm)
Swaroop Ghosh - *Univ. of South Florida, Tampa, FL*

50 PREDICTING THE FUTURE: HIDING THE MEMORY BOTTLENECK WITH PREDICTABLE CACHES AND SCRATCHPADS

Room: 13AB
Embedded Software

TS

Memory has been the performance bottleneck not only in high-end computers but also in embedded systems. Unfortunately, cache architectures are typically designed for throughput-oriented applications, where being fast is important, rather than real-time applications, where being predictable is important. This session presents four different approaches to designing predicable memory systems while achieving high performance and low energy consumption.

Chair:
Yuko Hara-Azumi - *Nara Institute of Science and Technology, Ikoma, Japan*

50.1 Reconciling Real-Time Guarantees and Energy Efficiency Through Unlocked-Cache Prefetching (1:30pm)
Emilio Wuerges, Romulo de Oliveira, Luiz C.V. dos Santos - *Federal Univ.of Santa Catarina, Florianopolis, Brazil*

50.2 Integrated Instruction Cache Analysis and Locking in Multitasking Real-Time Systems (1:45pm)
Huping Ding - *National Univ. of Singapore, , Singapore*
Yun Liang - *Peking Univ., Beijing, China*
Tulika Mitra - *National Univ. of Singapore, , Singapore*

50.3 Precise Timing Analysis for Direct-Mapped Caches (2:00pm)
Sidharta Andalam - *TUM CREATE Ltd., Singapore*
Roopak Sinha, Partha Roop - *Univ. of Auckland, Auckland, New Zealand*
Alain Girault - *INRIA, Saint-Ismier, France*
Jan Reineke - *Univ. des Saarland, Saarbrücken, Germany*

50.4 SSDM: Smart Stack Data Management for Software Managed Multicores (SMMs) (2:15pm)
Jing Lu, Ke Bai, Aviral Shrivastava - *Arizona State Univ., Tempe, AZ*

51 ONE SMALL STEP FOR PLACEMENT, ONE BIG LEAP FOR ROUTABILITY!

Room: 14
Physical Design

"Houston, we have a routability problem." We have great solutions for you in Austin! The landscape of placement research has shifted significantly in recent years. The research community has realized that a pure wirelength objective does not solve the real physical design challenge. Routability has become a "must" in placement research. Watch the launch of the next generation of placement innovations.

Chair:
Paul Villarrubia - *IBM Corp., Austin, TX*

51.1 Taming the Complexity of Coordinated Place and Route (1:30pm)
Jin Hu, Myung-Chul Kim - *IBM Corp., Austin, TX*
Igor Markov - *Univ. of Michigan, Ann Arbor, MI*

51.2 Routability-Driven Placement for Hierarchical Mixed-Size Circuit Designs (1:45pm)
Meng-Kai Hsu, Yi-Fang Chen, Chau-Chin Huang - *National Taiwan Univ., Taipei, Taiwan*
Tung-Chieh Chen - *Synopsys, Inc., Hsinchu, Taiwan*
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

51.3 Ripple 2.0: High Quality Routability-Driven Placement via Global Router Integration (2:00pm)
Xu He, Tao Huang, Wing-Kai Chow, Jian Kuang, Ka Chun Lam, Wenzan Cai, Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong, Hong Kong*

51.4 Optimization of Placement Solutions for Routability (2:15pm)
Wen-Hao Liu - *National Chiao Tung Univ., Hsinchu, Taiwan*
Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*
Yih-Lang Li - *National Chiao Tung Univ., Hsin-Chu, Taiwan*

52 FROM CLASSICAL TO NOVEL EDA SYSTEMS

Room: 15
System Level Design and Communication

This session expands EDA to new domains and rethinks classical system design. This requires new approaches across multiple level of abstractions. The papers address this challenge through exploration with upgradeable cyber physical models of biological systems and through high level synthesis techniques. The session continues the 'out of the box' theme with papers on electrical energy storage systems and 3D memory systems.

Chair:
Dirk Stroobandt - *Ghent Univ., Ghent, Belgium*

52.1 Exploration with Upgradeable Models Using Statistical Methods for Physical Model Emulation (1:30pm)
Bailey Miller, Frank Vahid - *Univ. of California, Riverside, CA*
Tony Givargis - *Univ. of California, Irvine, CA*

52.2 Modular System-Level Architecture for Concurrent Cell Balancing (1:45pm)
Matthias Kauer, Swaminathan Narayanaswami, Sebastian Steinhorst, Martin Lukasiewycz - *TUM CREATE Ltd., Singapore*
Samarjit Chakraborty - *Technical Univ. of Munich, Munich, Germany*
Lars Hedrich - *Univ. of Frankfurt, Frankfurt, Germany*

52.3 A Method to Abstract RTL IP Blocks into C++ Code and Enable High-Level Synthesis (2:00pm)
Nicola Bombieri - *Univ. of Verona, Verona, Italy*
Hung-Yi Liu - *Columbia Univ., New York, NY*
Franco Fummi - *Univ. of Verona, Verona, Italy*
Luca Carloni - *Columbia Univ., New York, NY*

52.4 DMR3D: Dynamic Memory Relocation in 3D Multicore Systems (2:15pm)
Dean Ancajas, Koushik Chakraborty, Sanghamitra Roy - *Utah State Univ., Logan, UT*

TS

54 PANEL: CYBER-PHYSICAL SYSTEM SOFTWARE: EMPEROR'S NEW CLOTHES OR NOT?

Room: 16AB
Embedded Software

The term "cyber-physical systems (CPS)" is currently one of the hottest technical terms. It was introduced in order to express a view on systems—such as cars, buildings and the smart grid—which is wider than that on traditional embedded systems. This widening includes the modeling of the physical environment and the linking of embedded systems through the use of network-based communications. One question about cyber-physical systems pops up immediately: What is new for cyber-physical systems? More in particular: What is new for cyber-physical system software?

Moderator:
Peter Marwedel - *Technische Univ. Dortmund, Dortmund, Germany*

Panelists:
Karl-Erik Arzen - *Lund Univ., Lund, Sweden*
Marco Di Natale - *Scuola Superiore Sant'Anna, Pisa, Italy*
Rolf Ernst - *Technische Univ. Braunschweig, Braunschweig, Germany*
Rajesh Gupta - *Univ. of California at San Diego, La Jolla, CA*
Rob Oshana - *Freescale Semiconductor, Inc., Austin, TX*

SESSION 60: SKY TALK: 5:00 - 5:30PM
On the Convergence of Mainstream and Mission Critical Markets

55 SPECIAL SESSION: POWERING HETEROGENEOUS SOCS AT THE RIGHT PLACE AND RIGHT TIME

Room: 12AB
Low-Power Design and Power Analysis

Heterogeneous systems on chip are here. Power distribution and delivery in both space and time for heterogeneous SoCs play a major role in designing low-power heterogeneous SoCs. Increasing chip complexity, demanding low-power requirements, diverse functionalities, and emerging integration technologies present tremendous challenges. Overcoming such challenges needs orchestrated efforts at various fronts. This session presents some recent work from both industry and academia towards tackling these challenges. The talks will cover advanced power management techniques across the product range from high performance CPU and GPU to ultra-low-power embedded processors, cutting-edge design of power switches to provide rapid changes in the energy-speed operating point to match workloads, and methodologies and tools for designing power distribution network in 3D stacked systems.

Chair:
Naehyuck Chang - *Seoul National Univ., Seoul, Republic of Korea*

55.1 Power Gating Applied to MP-SoCs for Standby-Mode Power Management (3:30pm)
David Flynn - *ARM, Ltd., Cambridge, United Kingdom*

55.2 Power Management and Delivery for High-Performance Microprocessors (4:00pm)
Tanay Karnik, Mondira (Mandy) Pant, Shekhar Borkar - *Intel Corp., Hillsboro, OR*

55.3 Flexible On-Chip Power Delivery for Energy Efficient Heterogeneous Systems (4:30pm)
Benton Calhoun, Kyle Craig - *Univ. of Virginia, Charlottesville, VA*

55.4 Power and Signal Integrity Challenges in 3D Systems (5:00pm)
Miguel Miranda Corbalan - *Qualcomm, Inc., Brussels, Belgium*
Anup Keval, Thomas Toms, Durodami Lisk, Rico Radojcic, Matt Nowak - *Qualcomm Technologies, Inc., San Diego, CA*

56 AGE OF FLASH

Room: 11AB
Embedded Architecture & Platforms

While NAND flash is being increasingly employed by embedded and high-end systems, they pose challenging issues from performance, reliability, power and space management angles. These challenges are compounded by the current trend towards volatile storage structures. This session covers all these issues by pointing specific problems, giving innovative solutions and discussing future applications.

Chair:
Hai Li - *Univ. of Pittsburgh, Pittsburgh, PA*

56.1 Underpowering NAND Flash: Profits and Perils (3:30pm)
Hung-Wei Tseng, Laura Grupp, Steven Swanson - *Univ. of California at San Diego, La Jolla, CA*

56.2 New ERA: New Efficient Reliability-Aware Wear Leveling for Endurance Enhancement of Flash Storage Devices (3:45pm)
Ming-Chang Yang - *National Taiwan Univ., Taipei, Taiwan*
Yuan-Hao Chang, Che-Wei Tsao - *Academia Sinica, Taipei, Taiwan*
Po-Chun Huang - *National Taiwan Univ., Taipei, Taiwan*

56.3 SAW: System-Assisted Wear Leveling on the Write Endurance of NAND Flash Devices (4:00pm)
Chundong Wang, Weng-Fai Wong - *National Univ. of Singapore, , Singapore*

56.4 Performance Enhancement of Garbage Collection for Flash Storage Devices: An Efficient Victim Block Selection Design (4:15pm)
Che-Wei Tsao, Yuan-Hao Chang, Ming-Chang Yang - *Academia Sinica, Taipei, Taiwan*

56.5 DuraCache: A Durable SSD Cache Using MLC NAND Flash (4:30pm)
Ren-Shuo Liu, Chia-Lin Yang, Cheng-Hsuan Li, Geng-You Chen - *National Taiwan Univ., Taipei, Taiwan*

57 WHY DOES CONSTRAINT-DRIVEN DESIGN MATTER FOR MULTICORE EMBEDDED SYSTEMS?

Room: 13AB
Embedded Design Methodologies

TS

Satsfying design constraints becomes more pressing when dealing with a large number of cores. This session addresses relevant challenges for the design of multiple-constraint-driven multicore embedded systems. How can we guarantee distributed stable states of process networks? How can we manage resources efficiently at run time? How can we estimate and guarantee real-time performance at design time? How can we build virtual platforms? How can we schedule tasks efficiently at design time?

Chair:
Hyunok Oh - *Hanyang Univ., Seoul, Republic of Korea*

57.1 Distributed Stable States for Process Networks - Algorithm, Analysis, and Experiments on the Intel SCC (3:30pm)
Devendra Rai, Lars Schor, Nikolay Stoimenov, Lothar Thiele - *Eidgenössische Technische Hochschule Zürich, Zurich, Switzerland*

57.2 Distributed Run-Time Resource Management for Malleable Applications on Many-Core Platforms (3:45pm)
Iraklis Anagnostopoulos, Vasileios Tsoutsouras, Alexandros Bartzas, Dimitrios Soudris - *National Technical Univ. of Athens, Athens, Greece*

57.3 netShip: A Networked Virtual Platform for Large-Scale Heterogeneous Distributed Embedded Systems (4:00pm)
YoungHoon Jung - *Columbia Univ., New York, NY*
Jinhyung Park - *Thing Daemon, LLC, New York, NY*
Michele Petracca - *Cadence Design Systems, Inc., San Jose, CA*
Luca Carloni - *Columbia Univ., New York, NY*

57.4 Exploiting Just-Enough Parallelism when Mapping Streaming Applications in Hard Real-Time Systems (4:15pm)
Jiali Teddy Zhai, Mohamed Bamakhrama, Todor Stefanov - *Leiden Univ., Leiden, The Netherlands*

57.5 On Robust Task-Accurate Performance Estimation (4:30pm)
Yang Xu, Bo Wang, Ralph Hasholzner - *Intel Corp., Neubiberg, Germany*
Rafael Rosales, Juergen Teich - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*

57.6 Stochastic Response-Time Guarantee for Non-Preemptive, Fixed-Priority Scheduling Under Errors (4:45pm)
Philip Axer, Rolf Ernst - *Technische Univ. Braunschweig, Braunschweig, Germany*

58 SYSTEM DESIGN WITH POWER AND THERMAL CONSTRAINTS

Room: 14
Low-Power Design and Power Analysis

From chip multiprocessors to data centers with thousands of nodes, power and thermal constraints remain as severe challenges in computer system design.

This session consists of six papers that propose novel solutions in system management and architectural optimization. The session starts with solutions targeting dark silicon and power management of many-core systems. The following presentations propose power budgeting and temperature-aware workload management methods for data centers, GPGPUs, and 3D stacked systems.

Chair:
John Sartori - *Univ. of Minnesota, Twin Cities, Minneapolis, MN*

58.1 HaDeS: Architectural Synthesis for Heterogeneous Dark Silicon Chip Multi-processors (3:30pm)
Yatish Turakhia - *Indian Institute of Technology, Mumbai, India*
Bharathwaj Raghunathan, **Siddharth Garg** - *Univ. of Waterloo, ON, Canada*
Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

58.2 Hierarchical Power Management for Asymmetric MultiCore in Dark Silicon Era (3:45pm)
Thannirmalai Somu Muthukaruppan, Mihai Pricopi, Vanchinathan Venkataramani, Tulika Mitra - *National Univ. of Singapore, , Singapore*
Sanjay Vishin - *CSR, Sunnyvale, CA*

58.3 Peak Power Reduction and Workload Balancing by Space-Time Multiplexing based Demand-Supply Matching for 3D Thousand-Core Microprocessor (4:00pm)
Kanwen Wang, **Sai Manoj P D**, Hao Yu - *Nanyang Technological Univ., Singapore*

58.4 Techniques for Energy-Efficient Power Budgeting in Data Centers (4:15pm)
Xin Zhan, Sherief Reda - *Brown Univ., Providence, RI*

58.5 Temperature Aware Thread Block Scheduling in GPGPUs (4:30pm)
Rajib Nath - *Univ. of California at San Diego, La Jolla, CA*
Raid Ayoub - *Intel Corp., Hillsboro, OR*
Tajana Simunic Rosing - *Univ. of California at San Diego, La Jolla, CA*

58.6 VAWOM: Temperature and Process Variation Aware WearOut Management in 3D Multicore Architectures (4:45pm)
Hossein Tajik - *Univ. of California, Irvine, CA*
Houman Homayoun - *George Mason Univ., Fairfax, VA*
Nikil Dutt - *Univ. of California, Irvine, CA*

59 GOT YIELD PROBLEMS? TAKE A CLOSER LOOK AT VARIABILITY AND RELIABILITY!

Room: 15
Verification and Simulation

TS

3D ICs is a hope for future SOC, but reliability remains a severe challenge. This session shows that power delivery becomes easier with a dedicated tier of DC-DC converters. 3D IC designers will learn how to extract TSV-to-TSV coupling parasitics. TSV-induced mechanical stress leads to cracks and other structural damage, so accurate analysis is a must. Classical problems of variability are not forgotten here. The performance of SSTA is dramatically improved with smart statistical min/max computations. Approximate computation eliminates timing problems in logic synthesis. Variation is not always an enemy but can be our friend when we design unclonable circuits.

Chair:
David Newmark - *Advanced Micro Devices, Inc., Austin, TX*

59.1 On the Potential of 3D Integration of Inductive DC-DC Converter for High-Performance Power Delivery (3:30pm)
Sergio Carlo, Wen Yueh, Saibal Mukhopadhyay - *Georgia Institute of Technology, Atlanta, GA*

59.2 Full-Chip Multiple TSV-to-TSV Coupling Extraction and Optimization in 3D ICs (3:45pm)
Taigon Song - *Georgia Institute of Technology, Atlanta, GA*
Chang Liu - *Broadcom Corp., Irvine, CA*
Yarui Peng, Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

59.3 An Accurate Semi-Analytical Framework for Full-Chip TSV-Induced Sztress Modeling (4:00pm)
Yang Li, David Pan - *Univ. of Texas at Austin, TX*

59.4 Speeding up Computation of the max/min of a set of Gaussians for Statistical Timing Analysis and Optimization (4:15pm)
Vimitha Kuruvilla, **Debjit Sinha**, Jeff Piaget, Chandu Visweswariah - *IBM Systems and Technology Group, East Fishkill, NY*
Nitin Chandrachoodan - *Indian Institute of Technology, Madras, India*

59.5 InTimeFix: A Low-Cost and Scalable Technique for In-Situ Timing Error Masking in Logic Circuits (4:30pm)
Feng Yuan, Qiang Xu - *The Chinese Univ. of Hong Kong, Hong Kong*

59.6 Improving PUF Security with Regression-Based Distriller (4:45pm)
Chi-En Yin, **Gang Qu** - *Univ. of Maryland, College Park, MD*

▶1 PANEL: CLOUD SERVER WAR – EMBEDDED PROCESSOR BATTLEGROUND: AUSTIN

Hall 5
Designer Track

DT

Monday, June 3 - 1:30 - 3:00pm

Cloud computing is a fast growing market for data centers. But, it imposes new challenges to Server Chip architectures (such as low power, virtualization, security, embedded software compatibility to name a few). Austin is an embedded processor battleground. Let's hear how companies (using disruptive technologies) are going to tackle these new challenges and how cloud computing could change your lives. The panel will also have end users with the unique perspective of the role of embedded systems in the success for cloud storage, search, and computing.

Moderator:
J. Scott Gardner - *The Linley Group, Austin, TX*

Panelists:
MIke Flippo - *ARM, Inc., Austin, TX*
Robert Hormuth - *Dell Inc., Austin, TX*
Gary Lauterbach - *Advanced Micro Devices, Inc., Austin, TX*
Anil Sabbavarapu - *Intel Corp., Austin, TX*
Hunter Scales - *Applied Micro Circuits Corp., Austin, TX*
Dave Shippy - *Altera Corp., Austin, TX*

▶2 SYSTEM DESIGN APPROACHES

Room: 18C
Designer Track

Tuesday, June 4 - 10:30am - 12:00pm

Power consumption has become a key market differentiator for SoCs. Power directly affects battery life and thermal dissipation; both are key considerations for any device that uses the SoCs. Accurate power modeling enables optimization of energy usage and thermal dissipation: by design changes or by modifying the dynamic behavior of applications. In this session, power modeling is used to validate a thermal mitigation scheme, thermal sensors are used as input to a Linux kernel to provide dynamic power management, techniques are shown to reduce the space and time requirement for RTL power estimation while maintaining most of the accuracy, and a flow is presented to enable early power estimation based on IP-block power models.

Chair:
Jan Rellemeyer - *IBM Corp., Austin, TX*

2.1 HLS-Based HW and SW Co-Design of Complex IP Subsystems - An Integrated Modeling, Synthesis, and Verification Methodology (10:30am)
Xiaojian Liu, Greg Smith, **David Hansen**, Jeff Wong, Louie Lee - *Qualcomm, Inc., Markham, ON, Canada*

2.2 Synthesizable, Application-Specific NOC Generation using CHISEL (10:45am)
Maysam Lavasani - *Univ. of Texas at Austin, TX*
Eric Chung, John Davis - *Microsoft Research, Mountain View, CA*

2.3 Churning the Most out of IP-XACT for Superior Design Quality (11:00am)
Ayon Dey - *Texas Instruments India Pvt. Ltd., Bangalore, India*
Anshuman Nayak, Samantak Chakrabarti, Samiullah Shaik - *Atrenta Inc., Noida, India*

2.4 Scalability Achievement by Low-Overhead, Transparent Threads on an Embedded Many-Core Processor (11:15am)
Takeshi Kodaka, Akira Takeda, Shunsuke Sasaki, Akira Yokosawa, Toshiki Kizu, Takahiro Tokuyoshi, Hui Xu, Toru Sano, Hiroyuki Usui, Jun Tanabe, Takashi Miyamori, Nobu Matsumoto - *Toshiba Corp., Kawasaki, Japan*

▶3 POSTER SESSION 1 - (LISTING ON PAGES 40-41)

Tuesday, June 4 - 12:00 - 1:30pm

Hall 5
Designer Track

▶4 BACK-END FLOWS AND METHODOLOGIES

Room: 18C
Designer Track

Tuesday, June 4 - 1:30 - 3:00pm

Expert designers typically find that the quality of flows/methodologies is equally important to the quality of back-end tools (if not more important). This is because the methodology often defines and limits what and how the tool works in each step. In this session, two presentations improve the design methodology in terms of QoR, TAT and productivity. The other presentations cover an EDA data-mining tool and a clock-tree synthesis methodology.

Chair:
Rajarshi Ray - *Broadcom Corp., Pflugerville, TX*

4.1 A Smarter Design Environment (1:30pm)
Tom Guzowski - *IBM Corp., Essex, VT*

4.2 Impromptu Data Extraction and Analysis (1:45pm)
Sandeep Patwari, Anand Ananthanarayanan - *Intel Corp., Bangalore, India*

4.3 Methodology for High-Speed Clock Tree Implementation in Large, High-Performance Chips (2:00pm)
Ravi Rachala, Aaron Grenat, Prashanth Vallur, Chris Ang - *Advanced Micro Devices, Inc., Austin, TX*

4.4 A Quality-Driven Physical Implementation Flow (2:15pm)
Gokhan Isik, Umut Eksi, Arzu Datli - *Ericsson, Istanbul, Turkey*

5 NEW USES OF FORMAL METHODS

Room: 18C
Designer Track

Tuesday, June 4 - 4:00 - 6:00pm

DT

Formal and Assertion-Based Verification is increasingly seen as an essential design technology: enabling verification of equivalence between RTL and schematics and high-confidence validation of RTL spec compliance. However, it is also expanding beyond its traditional niches, enabling new usage models that are changing the ways processors and SoCs are designed and validated. This session covers a variety of formal-based approaches.

Chair:
Andy Martin - *IBM Research - Austin, Austin, TX*

5.1 Using Formal Verification to Replace Mainstream Simulation (4:00pm)
Erik Seligman, Brandon Smith - *Intel Corp., Hillsboro, OR*

5.2 Automatic Verification of Dependency (4:15pm)
Xiushan Feng - *NVIDIA Corp., Austin, TX*
Jay Bhadra - *Freescale Semiconductor, Inc., Austin, TX*

5.3 Assertion-Based Design Partition (4:30pm)
Xiushan Feng - *NVIDIA Corp., Austin, TX*
Jay Bhadra, Ross Patterson - *Freescale Semiconductor, Inc., Austin, TX*

5.4 Automated Method Eliminates X Bugs in RTL and Gates (4:45pm)
Kai-hui Chang, Yen-ting Liu, Chris Browy - *Avery Design Systems, Inc., Andover, MA*

5.5 Automatic Verification of Floating Point Units (5:00pm)
Udo Krautz, Viresh Paruthi - *IBM Systems and Technology Group, Austin, TX*
Anand Arunagiri, Sujeet Kumar - *IBM Server and Technology Group, Bangalore, India*

5.6 FreescaleADL: An Industrial-Strength Architectural Description Language For Programmable Cores (5:15pm)
Brian Kahne - *Freescale Semiconductor, Inc., Austin, TX*

6 SYSTEM POWER ESTIMATION AND PERFORMANCE VERIFICATION

Room: 18C
Designer Track

Wednesday, June 5 - 9:00 - 10:30am

As design complexity grows, design methodologies and approaches must keep up in order to enable timely execution and high-quality designs. In this session, high-level synthesis is used to perform HW/SW co-design, a new NoC generator is used for power efficient interconnect design exploration, an approach is described for utilizing IP-XACT to automate checking and help verification, and a scalable parallel processing scheme is applied to a 32-core processor.

Chair:
Debashis Bhattacharya - *Huawei Technologies Co., Ltd., Plano, TX*

6.1 Early Validation of MPSoCs Thermal Mitigation through Integration of Thermal Simulation in SystemC Virtual Prototyping (9:00am)
Tanguy Sassolas, Charly Bechara - *CEA-LIST, Gif-sur-Yvette, France*
Pascal Vivet - *CEA-LETI, Grenoble, France*
Hela Boussetta - *DOCEA Power, Inc., Moirans, France*
LUCA FERRO - *TIMA Labs, GRENOBLE, France*

6.2 Design of Optimal Closed Loop Controller and OS Scheduler for Dynamic Energy Management in Heterogeneous Multicore Processors (9:15am)
Vinay Hanumaiah, Digant Desai, Sarma Vrudhula - *Arizona State Univ., Tempe, AZ*

6.3 Critical Signal Flow for Power Estimation: The Road to Billion Gate SoC Power Verification (9:30am)
Chungki Oh, Jianfeng Liu, Seokhoon Kim, Kyung-Tae Do, Jung Yun Choi, Hyo-Sig Won, Kee Sup Kim - *Samsung, Yongin, Republic of Korea*
Jeongwon Kang - *ANSYS, Inc, Seoul-City, Republic of Korea*
Kamlesh Madheshiya - *Sequence Design, Inc., Noida, India*
Arti Dwivedi - *ANSYS, Inc, Singapore*

6.4 Power Modeling Flow for a Power Analysis at the System Level (9:45am)
Cyril Chevalier, Audrey Le-Clercq - *STMicroelectronics, Grenoble, France*
Philippe Garrault - *DOCEA Power, Inc., Moirans, France*

7 POSTER SESSION 2 - (LISTING ON PAGES 42-43)

Wednesday, June 5 - 12:00 - 1:30pm

Hall 5
Designer Track

8 SIMULATION AND EMULATION

Room: 18C
Designer Track

Wednesday, June 5 - 1:30 - 3:00pm

Simulation and emulation continue to be the primary technologies for pre-Silicon logic validation. In this session, we will hear about design experiences with methods that optimize the usage of these techniques. These ideas promise to enable more efficient validation that requires less human effort, while enabling design and validation engineers to find more bugs.

Chair:
Erik Seligman - *Intel Corp., Hillsboro, OR*

8.1 Optimization of Verification Effort Using Reusable Sequences (1:30pm)
Gaurav Chugh, Dipesh Handa, Gaurav Minda, Kumar Ranjan - *Synopsys (India) Pvt. Ltd., New Delhi, India*

8.2 Enabling Easy Creation of HW Reconfiguration Scenarios for System-Level, Pre-Silicon Simulation (1:45pm)
Erez Bilgory, **Tali Rabetti**, Ronny Morad, Alex Goryachev - *IBM Haifa Research Lab., Haifa, Israel*

8.3 Regression Optimization Using Hierarchical Jaccard Similarity and Machine Learning (2:00pm)
Monica Farkash, Bryan Hickerson - *IBM Systems and Technology Group, Austin, TX*

8.4 Parallel Design Methodology for Video Codec LSI with High-Level Synthesis and FPGA-Based Platform (2:15pm)
Kazuya Yokohari, Koyo Nitta, Mitsuo Ikeda, Atsushi Shimizu - *Nippon Telegraph and Telephone Corp., Kanagawa, Japan*

▶9 DESIGNER KEYNOTE Q/A

Hall 5
Designer Track

DT

Wednesday, June 5 - 1:30 - 3:00pm

This special session is an interactive follow-up to the Wednesday morning Designer Track keynotes by Scott Runner (Qualcomm) and Sanjive Agarwala (Texas Instruments). Scott, Sanjive, and senior leaders from their design teams will sit for a joint question/answer panel session with the audience. Come take advantage of this unusual opportunity!

Moderator:
Robert Jones - *Intel Corp., Hillsboro, OR*

Panelists:
J. Scott Runner - *Qualcomm Technologies, Inc., San Diego, CA*
Matt Severson - *Qualcomm Technologies, Inc., Austin, TX*
Martin Saint-Laurent - *Qualcomm Technologies, Inc., Austin, TX*
Sanjive Agarwala - *Texas Instruments, Inc., Dallas, TX*
Anthony Hill - *Texas Instruments, Inc., Dallas, TX*
Tim Anderson - *Texas Instruments, Inc., Austin, TX*

▶10 PHYSICAL DESIGN AND MANUFACTURABILITY

Room: 18C
Designer Track

Wednesday, June 5 - 4:00 - 6:00pm

Yield and manufacturability has become one of the hottest topics in physical design because of its importance in advanced technology nodes. Presentations in this session include designer experiences with a flow to reduce hotspots, a hierarchical methodology for very high-frequency microprocessor designs, power distribution and clock-tree synthesis for large low-power ASIC chips, a flow to handle clock-domain crossing logics, and a top-down flow for 3D-IC designs.

Chair:
Rajesh Raina - *Freescale Semiconductor, Inc., Austin, TX*

10.1 Advanced Model-Based Hotspot Fix Flow for Layout Optimization with Genetic Algorithm (4:00pm)
Shuhei Sota - *Toshiba Microelectronics Corp., Yokohama, Japan*
Taiga Uno, Masanari Kajiwara, Chikaaki Kodama - *Toshiba Corp., Yokohama, Japan*
Hirotaka Ichikawa - *Toshiba Microelectronics Corp., Kawasaki, Japan*
Ryota Aburada, Toshiya Kotani - *Toshiba Corp., Yokohama, Japan*
Kei Nakagawa, Tamaki Saito - *Toshiba Microelectronics Corp., Kawasaki, Japan*

10.2 Use of Hierarchical Design Methodologies in Global Infrastructure of the POWER7+ Processor (4:15pm)
Brian Veraa, Ryan Nett, Ryan Kruse - *IBM Systems and Technology Group, Austin, TX*

10.3 Power Delivery Network Optimization for Low-Power SoC (4:30pm)
Anil Gundurao, Melinda (Ling) Yang, Eileen You, Harpreet Gill - *Samsung, San Jose, CA*

10.4 Systematic Method for Capturing "Design Intent" of Clock Domain Crossing (CDC) Logic in Constraints (4:45pm)
Ramesh Rajagopalan, Ajay Bhandari - *Cisco Systems, Inc., San Jose, CA*

10.5 Path-Finding Methodology for Interposer and 3D Die Stacking (5:00pm)
Sherry Xiaoxia Wu - *Qualcomm Technologies, Inc., San Jose, CA*
Ravi Varadarajan, Navneet Mohindru - *Atrenta Inc., San Jose, CA*
Durodami Lisk, Riko Radojcic - *Qualcomm, Inc., San Diego, CA*

10.6 A Clock Tree Synthesis Flow Tailored For Low Power
Arzu Datli, Umut Eksi, Gokhan Isik - *Ericsson, Istanbul, Turkey*

▶11 PHYSICAL DESIGN FOR MEMORY DESIGN AND NEW TECHNOLOGIES

Room: 18C
Designer Track

Thursday, June 6 - 9:00 - 10:30am

This session focuses on memory design methodologies and 3D ICs. First, a debug standard for 3D designs is presented. The other three talks cover incorporating physical-awareness into the memory BISR flow, snapback checking in a memory design flow, and SRAM test structures for improving yield.

Chair:
David Z. Pan - *Univ. of Texas at Austin, TX*

11.1 Standard-Based Instrumentation Schemes for 3D SoC (9:00am)
Neal Stollon - *HDL Dynamics, Dallas, TX*

11.2 Hierarchical, Physical-Aware, Built-In Self-Repair of Embedded Memories (9:15am)
Devanathan VR, Harsharaj Ellur, Mohd Imran, Shivani Bathla - *Texas Instruments India Pvt. Ltd., Bangalore, India*

11.3 Snapback Avoidance Design Flow for a Memory Technology (9:30am)
Wesley Kwong, Owen Jungroth, Magnolia Maestre, Sean McDermott, Karthik Srikanta Murthy - *Intel Corp., Santa Clara, CA*

11.4 Mini-SRAM Test Structures: Distributed SRAM Yield Micro Probes for Monitoring 3D Integrated Chips (9:45am)
Jente Kuang - *IBM Research, Austin, TX*
Keith Jenkins - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

12 ANALOG AND PHYSICAL ISSUES IN THE FRONT END

Room: 17AB
Designer Track

DT

Thursday, June 6 - 9:00 - 10:30am

Although front-end designers like to live in the ideal world presented by digital RTL modeling, many can no longer afford this luxury. It is increasingly important to include awareness of analog and other physical issues as early as possible in the design process. In this session we will hear about designer experiences with techniques that examine and verify analog and physical issues during the front-end phase of processor design.

Chair:
Ken Albin - *Intel Corp., Austin, TX*

12.1 Coverage-Driven Verification for Analog Design Based on UCIS (9:00am)
Atul Pandey, Marius Sida, Guido Clemens - *Mentor Graphics Corp., Munich, Germany*

12.2 How to Accelerate the Analog Design Verification Flow (9:15am)
Gabi Glasser - *Intel Corp., Jerusalem, Israel*
Itai Yarom - *Synopsys, Inc., Herzelia, Israel*

12.3 Single Event Upset Hardening by 'Hijacking' the Multi-VT Flow During Synthesis (9:30am)
Roland Weigand - *European Space Agency, Noordwijk, The Netherlands*

13 VIRTUAL PLATFORMS AND PROTOTYPING

Room: 18C
Designer Track

Thursday, June 6 - 1:30 - 3:00pm

High-level modeling methodologies now enable comprehensive modeling of a target system at acceptable levels of performance. Some methodologies can include a full OS and application stack. The wide scope and high simulation performance enables exploration of and solutions for a range of problems. The presentations in this session address the performance and functional verification of software, performance evaluation of new memory architectures, and the challenge of maintaining high levels of performance when mixing simulation environments.

Chair:
Alicia Strang - *Cadence Design Systems, Inc., Aliso Viejo, CA*

13.1 Filling the Gap Between System Design and Performance Verification (1:30pm)
Rafik Henia, Laurent Rioux, Nicolas Sordon - *Thales Group, Palaiseau, France*

13.2 Using Virtual Platforms for Firmware Verification (1:45pm)
James Pangburn, **Jason Andrews** - *Cadence Design Systems, Inc., Ham Lake, MN*

13.3 Virtual Platforms for Memory Controller Design Space Exploration (2:00pm)
Matthias Jung - *Univ. of Kaiserslautern, Kaiserslautern, Germany*
Christian Weis, Norbert Wehn - *Technische Univ. Kaiserslautern, Kaiserslautern, Germany*

13.4 Simics SystemC Hybrid Virtual Platform - A Case Study (2:15pm)
Asad Khan - *Intel Corp., Chandler, AZ*

14 PHYSICAL SYNTHESIS TOOLS AND TECHNIQUES

Room: 17AB
Designer Track

Thursday, June 6 - 1:30 - 3:00pm

As interconnect delays dominate chip timing and performance, physical synthesis becomes more critical to the overall design flow. In this session, different physical synthesis techniques are demonstrated: closing the gap between ASIC and microprocessors, a flow for critical path monitors, and power reduction structures and flows.

Chair:
Yaping Zhan - *Advanced Micro Devices, Inc., Austin, TX*

14.1 Structured Synthesis Techniques Applied to a Dataflow Macro (1:30pm)
Mani Viswanath - *IBM Corp., Austin, TX*
Matthew Ziegler - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

14.2 Accurate Model-to-Hardware Simulation Methodology for Designing Critical Path Monitors over a Wide Voltage Range (1:45pm)
Alan Drake - *IBM Research - Austin, TX*
Xiaobin Yuan, Pawel Owczarczyk, Marshall Tiner - *IBM Systems and Technology Group, Austin, TX*

14.3 POWER Synthesis: The Transition from Custom Circuit Design to Large Block Synthesis in a High-Performance Environment (2:00pm)
Jeff Brownscheidle, Maureen Delaney, Eric Fluhr, Pat Mcilmoyle, Tien Tran - *IBM Systems and Technology Group, Austin, TX*

14.4 Post RTL Structures/Flows Targeting Low Power in Intel Designs (2:15pm)
Srinivas Jammula, Ambar Mukherji, Naveen Kumar - *Intel Corp., Bengaluru, India*

▶15 POWER AND PERFORMANCE

Room: 18C
Designer Track

DT

Thursday, June 6 - 3:30 - 5:30pm

In modern chip design, power and performance are key factors determining success in the marketplace. While many off-the-shelf tools perform verification in these areas, there are still challenges in verifying power and performance correctly and efficiently at the earliest possible project stages. The presentations in this session focus on design experiences with techniques for validating and optimizing power/performance as part of the front-end RTL design process.

Chair:
John O'Leary - *Intel Corp., Hillsboro, OR*

15.1 Methodology for Effective Hierarchical Verification of Low-Power Designs (3:30pm)
Ramesh Rajagopalan - *Cisco Systems, Inc., San Jose, CA*
Namit Gupta - *Synopsys, Inc., Mountain View, CA*

15.2 Advanced Low-Power Verification Using Voltage Aware Models (3:45pm)
Mohit Jain, Ankita Arya - *STMicroelectronics, Greater noida, India*
Pierre-Yves Alla - *Synopsys, Inc., MontBonnot, France*

15.3 Performance Modeling and Validation of C66x DSP Multilevel Cache Memory System (4:00pm)
Rama Venkatasubramanian, Pete Hippleheuser, Oluleye Olorode, Abhijeet Chachad, Dheera Balasubramanian, Naveen Bhoria, Jonathan Tran, Hung Ong, David Thompson - *Texas Instruments, Inc., Dallas, TX*

15.4 Enabling Power-Aware Emulation in Big CPU Project (4:15pm)
Adriana Wolffberg, Neiroukh Osama, Vaddepalli Vinay - *Intel Corp., Zikhron Yaakov, Israel*

15.5 Design and Post-Optimization Flow for Advanced Thermal Management by use of Body Bias (4:30pm)
Hyung-Ock Kim, Jun Seomun, Jaehan Jeon, Chungki Oh, Wook Kim, Kyung-Tae Do, Jung Yun Choi, Hyo-Sig Won, Kee Sup Kim - *Samsung, Yongin, Republic of Korea*

15.6 Partial State Retention Verification - Challenges and Techniques (4:45pm)
Yushi Tian - *Broadcom Corp., San Diego, CA*
Amir Nilipour, Ajay Thiriveedhi - *Synopsys, Inc., Mountain View, CA*

▶16 INTERCONNECT SIMULATION AND ANALYSIS

Room: 17AB
Designer Track

Thursday, June 6 - 3:30 - 5:30pm

Interconnect simulation and analysis has long been one of the biggest challenges during backend flows because of its importance in design closure. This session includes presentations about chip/package co-simulation, power distribution analysis, double-patterning-aware extraction, inductor design for high-frequency clock networks, waveform distortion consideration during timing analysis, and multi-corner signoff analysis for large ASICs.

Chair:
Rajendran Panda - *Oracle Corp., Austin, TX*

16.1 Design Considerations and Improvement by Using Chip and Package Co-Simulation (3:30pm)
Yeong-Jar Chang - *Faraday Technology Corp., Hsinchu, Taiwan*

16.2 System-Level PDN Analysis Enhancement Including I/O Subsystem Noise Modeling (3:45pm)
Cornelia Golovanov, Rich Laubhan - *LSI Corp., Fort Collins, CO*
Chris Ortiz - *Apache Design, Inc. a subsidiary of ANSYS, Inc., San Jose, CA*

16.3 Double Patterning-Aware Extraction and Static Timing Analysis Flows For Digital Design Sign-Off in 20/14nm (4:00pm)
Tamer Ragheb, Steven Chan, Adrian Au Yeung, Richard Trihy - *GLOBALFOUNDRIES, Milpitas, CA*

16.4 Inductor Design for Global Resonant Clock Distribution (4:15pm)
Visvesh Sathe - *Advanced Micro Devices, Inc., Fort Collins, CO*

16.5 Timing Analysis With Waveform Propagation (4:30pm)
Moon Su Kim, Sunik Heo, DalHee Lee, DaeJoon Hyun, Kim Byung-Su, Bonghyun Lee, Chul Rim, Hyo-Sig Won, Kee Sup Kim - *Samsung, Yongin, Republic of Korea*

16.6 Fast, Efficient and Scalable Multi-Corner SoC Signoff Analysis Extension With Programmable In-Situ Spice Level Analysis Capability (4:45pm)
Anjali Supekar, Mohita Batra, **Rakesh Gulati**, Shahabuddin Quershi, Hina Mushir, Prashant Pandey, Samant Paul, Seema Jaiswal - *STMicroelectronics, Greater Noida, India*

POSTER SESSION 1

Hall 5
Designer Track

DT

3.1 Advanced Voltage Binning Using Statistical Timing
Eric Foreman, Lance Pickup, Jeffrey Hemmett - *IBM Systems and Technology Group, Essex Junction, VT*
Vladimir Zolotov - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

3.2 Model-to-Hardware Correlation Using Statistical Timing
Eric Foreman, Stephen Shuma, Chris Parkinson, Anthony Fazekas - *IBM Systems and Technology Group, Research Triangle Park, NC*

3.3 Converged Statistical Timing Flow
Stephen Shuma, **Eric Foreman** - *IBM Systems and Technology Group, Essex Junction, VT*
Nathan Buck - *IBM Corp., Underhill, VT*
Michael Wood, Robert Allen, Chandu Visweswariah - *IBM Systems and Technology Group, East Fishkill, NY*

3.4 Peak Power Implications for Logic Designs and Avoiding Pit-Fall
Vinay Adavani - *Infinera Corp., Bangalore, India*

3.5 Low Power Static Checking Methodology now Integrated in MVRC
Neha Agarwal, **Neha Agarwal** - *STMicroelectronics, Greater Noida, India*
Patrick Blestel, Stephanie Varela - *Synopsys, Inc., Montbonnot Saint-Martin, France*
Luca Gerli - *STMicroelectronics, Crolles, France*

3.6 Methodology for Biomed-SW-HW Co-Design
Iyad Al Khatib, Edoardo Paone, Sotirios Xydis, Vittorio Zaccaria, Cristina Silvano - *Politecnico di Milano, Milano, Italy*

3.7 Implementation of a Multi-Threaded Network Stack on a Bare-Metal Embedded System
Kaiming Ho - *Fraunhofer IIS, Erlangen, Germany*

3.8 Profile-Based Architecture Power Modeling Methodology for AP/SoC Product
Jongho Kim, Myungkyoon Yim, Junghun Heo, Jianfeng Liu, Seokhoon Kim, Wook Kim, Kyung-Tae Do, Jung Yun Choi, Hyo-Sig Won, Kee Sup Kim - *Samsung, Yongin, Republic of Korea*
Samuel Amo, Hela Boussetta, Ridha Hamza - *DOCEA Power, Inc., Moirans, France*

3.9 Embedded Systems Realization with Hybrid Apps - Open Source ANDROID Meets Dynamic Partial Reconfiguration
Endric Schubert, David Epping - *Missing Link Electronics, Inc., Neu-Ulm, Germany*
Fabian Zentner - *Univ. of Ulm, Ulm, Germany*

3.10 Simplified Approach to On-Die Power and Signal Co-Simulation
Anand Ananthanarayanan, Srikanth Balasubramanian, Srikrishnan Venkataraman, David Ayers - *Intel Corp., Santa Clara, CA*

3.11 AMD Custom Design Methodology
Christopher Ang, David Newmark - *Advanced Micro Devices, Inc., Austin, TX*

3.12 Generating Efficient Reusable Testcases for a Family of Cores
Abi Asojo, Avinash Munshi, Jonathan Gamoneda - *Freescale Semiconductor, Inc., Austin, TX*

3.13 Static Low-Power Verification in Mixed-Signal SoC Designs
Shubhyant Chaturvedi - *Advanced Micro Devices, Inc., Austin, TX*
Pascal Bolzhauser - *Concept Engineering GmbH, Freiburg, Germany*
Shruti Anand - *Mentor Graphics Corp., Austin, TX*

3.14 Static Verification Methodology for Power Switch Network
Ankush Bagotra, Vishwanath Sundararaman, Pankaj Khandelwal - *Synopsys (India) Pvt. Ltd., Bangalore, India*
Animesh Jain - *NVIDIA Corp., Bangalore, India*

3.15 Static Verification Methodology for Bias Supply Network
Frederic Saint-Preux - *STMicroelectronics, Grenoble, France*
Ankush Bagotra, Neha Bajaj - *Synopsys (India) Pvt. Ltd., Bangalore, India*
Rohit Jain - *Synopsys, Inc., Bangalore, India*
Vishwanath Sundararaman - *Synopsys (India) Pvt. Ltd., Hyderabad, India*
David Salmon, Patrick Blestel - *Synopsys, Inc., Rungis, France*

3.16 Applying DOE to Logic Synthesis and Placement
Ethan Bancala - *Advanced Micro Devices, Inc., Boxborough, MA*

3.17 Graph-Based Verification Patterns
Jörg Behrend - *IBM Systems and Technology Group, Boeblingen, Germany*
Gero Dittmann - *IBM Research - Zurich,, Switzerland*
Klaus Keuerleber - *IBM Server and Technology Group, Boeblingen, Germany*
Joerg Grosse, Frederic Krampac - *Breker Verification Systems, Inc., San Jose, CA*

3.18 An Automation Approach to Generate LVS Regression Testcases in Custom Design Flow
Anshu Jain, Bhawna Tomar - *Intel Corp., Bangalore, India*

3.19 Watermarking Techniques for Protection of Soft IP Cores
Vikas Billa - *Tech Vulcan India Pvt Ltd.*
Sasikala Nellutla, Sai Chaithanya Palepu - *Kamala Institute of Technology and Science, Karimnagar, India*

3.20 Smarter, Greener Systems with Superior Productivity and Increased Predictability Using Dynamic Power Analysis
Jingbo Gao, Bing Zhu, **Raghu Binnamangalam** - *Cadence Design Systems, Inc., San Jose, CA*

3.21 Fabric Verification Using an Advanced Graph-Based Solution
Galen Blake - *Altera Corp., Austin, TX*
Mark Olen - *Mentor Graphics Corp., Wilsonville, OR*

3.22 Post-Clock Design Closure
Bertram Bradley, Bill Dougherty - *IBM Systems and Technology Group, Pittsburgh, PA*
Gregory Ford - *IBM Server and Technology Group, San Jose, CA*
Zhuo Li - *IBM Research - Austin, TX*

3.23 CPF: Getting SoC Power Configurations Right
Mike Brady - *Freescale Semiconductor, Inc., Austin, TX*

3.24 Using Automatic Path Pruning for Characterization and Timing Verification
Ethan Howe, **Lyren Brown**, Yoshiharu Kawamura, David Newmark - *Advanced Micro Devices, Inc., Austin, TX*

3.25 Array Timing and Power Validation Without Instantiated Netlist
Kevin Bercaw, Pranav Kumar Cherupalli, Eric Foreman, Christopher Ro - *IBM Systems and Technology Group, Essex Junction, VT*

3.26 QA Flows for DFM Using Open Standards
Gerald Buurma - *Silicon Integration Initiative, Inc., San Jose, CA*
Angela Johnson, **Marco Facchini** - *IBM Corp., East Fishkill, NY*

3.27 Automation and Results of a Volume Diagnosis Flow
Scott Guisinger, Dawei Pan - *Freescale Semiconductor, Inc., Austin, TX*

3.28 Margining with Advanced On-Chip Variation
Brian Cline, Jim Shiffer, Lena Ahlen-Gross - *ARM, Inc., Austin, TX*
Ahran Dunsmoor - *CLK Design Automation, Inc., Littleton, MA*

POSTER SESSION 1 *(CONTINUED)*

3.29 Cross Bar Message Network Protocol Bridge Verification Using Formal Methodology
Tushar Kanti Biswas, Bijitendra Mittra - *Interra Systems, Inc., Cupertino, CA*
Subir Roy, Subrangshu Das - *Texas Instruments India Pvt. Ltd., Bangalore, India*

3.30 Verification of Hardware Scheduler in a Multimedia Accelerator through Formal Methodology
Jayanta Ghosh, **Tushar Kanti Biswas**, Bijitendra Mittra - *Interra Systems, Inc., Cupertino, CA*
Subir Roy, Subrangshu Das - *Texas Instruments India Pvt. Ltd., Bangalore, India*

3.31 Automated Constraint Generation and Phase Engineering Methodology
Brian Dreibelbis - *IBM Corp., Underhill, VT*
Eric Foreman - *IBM Systems and Technology Group, Essex Junction, VT*
Nathan Buck - *IBM Corp., Underhill, VT*
John Dubuque, Lance Pickup - *IBM Systems and Technology Group, Raleigh, NC*

3.32 Co SI-PI Signoff on High-Speed DDR3 PHY Interface
Sandeep Dwivedi, Kishan Chanumolu, Nidhir Kumar - *ARM, Ltd., Bangalore, India*
Sankar Ramachandran, Vishnu Raj - *Apache Design, Inc. a subsidiary of ANSYS, Inc., Bangalore, India*

3.33 Cascading Power Management (Or, How to Beat DVFS in Advanced Process Technologies)
Ben Eckermann - *Freescale Semiconductor, Inc., Austin, TX*

3.34 Reliability by Design - Balancing Reliability, Complexity, and Verification
Adrian Evans, Dan Alexandrescu, Enrico Costenaro, Olivier Lauzeral - *iRoc Technologies, Mountain View, CA*

3.35 Optimization of Analog Integrated Circuits Using Surrogate Modeling
Yengui Firas - *Lyon Institute of Nanotechnology, Villeurbanne, France*

3.36 Power DV Methodology for 28nm SoC
Deepa Singh, **Jose Flores**, Steven Mullinnix - *Texas Instruments, Inc., Dallas, TX*

3.37 Automation of Power Intent through CPF for Low-Power Designs
Jose Flores - *Texas Instruments, Inc., Dallas, TX*
Kaijian Shi - *Cadence Design Systems, Inc., Plano, TX*
Anthony Hill - *Texas Instruments, Inc., Dallas, TX*

3.38 OSI-Based Protocols Verification – Demystifying and Mitigating Challenges
Parag Goel - *Synopsys (India) Pvt. Ltd., Bangalore, India*
Amit Sharma - *Synopsys, Inc., Pune, India*

3.39 Lending a 'Formal' Hand to CDC Verification: A Case Study of Non-Intuitive Failure Signatures
Vaishnav Gorur, Roger Hughes, James Moore - *Real Intent, Inc., Sunnyvale, CA*

3.40 Optimizing Distributed Computing Environment for Library Characterization
Michael Hale - *IBM Corp., Raleigh, NC*
William Wright, James Sundquist, Amol Joshi, Bob Maier - *IBM Systems and Technology Group, Hopewell Junction, NY*

3.41 Practical Consideration in a Sequential Power Optimization Flow
Udupi Harisharan - *Cisco Systems, Inc., San Jose, CA*
Uday Das - *Calypto Design Systems, Inc., San Jose, CA*

3.42 An IP-Centric Power-Aware Design Flow
David Hathaway - *IBM Systems and Technology Group, Burlington, VT*
Qi Wang - *Cadence Design Systems, Inc., San Jose, CA*
Nagu Dhanwada - *IBM Corp., Hopewell Junction, NY*
Jerry Frenkil - *Silicon Integration Initiative, Inc., Concord, MA*

3.43 Check-Based Approach to Abstracted Hierarchical Timing
Alex Rubin, David Hathaway, John Bannister, **Tim Helvey** - *IBM Systems and Technology Group, Rochester, MN*

3.44 Proven Implementation Techniques for 300+ Million Gate SoC Design
Koan Huang, Adrian Hung, Augusli Kifli, Kun-Cheng Wu - *Faraday Technology Corp., Hsinchu, Taiwan*

3.45 Macro Modeling-Based, Layout-Dependent Effect Aware Design Flow
Pei Yao, Rais Huda - *GLOBALFOUNDRIES, Milpitas, CA*
Philippe Hurat, Ajish Thomas - *Cadence Design Systems, Inc., San Jose, CA*
Grace Gao, Joe Louis-Chandran - *Rambus, Inc., Sunnyvale, CA*

3.46 A Sequential Equivalence Checking "App" Using Off-the-Shelf Formal Analysis Tools
Amy Yen - *NVIDIA Corp., Redmond, WA*
Darrow Chu - *Cadence Design Systems, Inc., San Jose, CA*

3.47 Find EDA Tools for a Faster Timing Closure With ECO and Clock-Path ECO
Anne Yue - *Synapse Design, Santa Clara, CA*

3.48 Rib-Based Routing for High Performance
Nancy Zhou - *IBM Corp., Cedar Park, TX*
Terrance Sehr, Gustavo Tellez, Peter Nasveschuk - *IBM Systems and Technology Group, Portland, ME*

POSTER SESSION 2

Hall 5
Designer Track

DT

7.1 Configurable Functional Coverage Model
Gaurav Chugh, Santosh Moharana, Apoorva Vats - *Synopsys (India) Pvt. Ltd., New Delhi, India*

7.2 Let us Broaden the UVM Horizon: A Proposal to Incorporate Standard Algorithms and Day-to-Day Verification Utilities in a Package
Anunay Bajaj - *Synopsys, Inc., Delhi, India*
Gaurav Chugh - *Synopsys (India) Pvt. Ltd., Delhi, India*

7.3 FAV - Verification Improved
Amil Kabil, **Ravi Prasad,** Bharathwaj Sankara - *Cisco Systems, Inc., San Jose, CA*

7.4 Multi-Threaded Statistical Static Timing Analysis on Multi-Million Instance 32nm Designs
Kerim Kalafala - *IBM Corp., Hopewell Junction, NY*
Eric Foreman, Chandu Visweswariah, Dileep Netrabile, Jeff Piaget - *IBM Systems and Technology Group, East Fishkill, NY*
Mark Lavin - *IBM Corp., Yorktown Heights, NY*
Jeffrey Hemmett - *IBM Systems and Technology Group, Essex Junction, VT*
Vladimir Zolotov - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Gregory Schaeffer, Jeffrey Staten, Steven Meyers - *IBM Systems and Technology Group, Williston, VT*

7.5 SOC Interconnect Analysis for Effective Verification, Architectural Exploration, and Post-Silicon Debug
Lalitha Bagepalli Shivaprakash, Kumaril Bhatt - *Marvell Semiconductor, Inc., Santa Clara, CA*
Nicholas Heaton, Bill Watt - *Cadence Design Systems, Inc., San Jose, CA*
Wenjia Liu - *Univ. of Michigan, Ann Arbor, MI*
Lilian Tran - *Stanford Univ., Stanford, CA*

7.6 Full Chip Metal/Via Filling Technique for Multi-Power Domains
Rajesh Karturi, Dibyendu Goswami - *Intel Corp., Bangalore, India*

7.7 Improving Design Productivity With a new Routing-Aware Physical Synthesis Flow
Michael Kazda - *IBM Systems and Technology Group, Hopewell Junction, NY*
Lakshmi Reddy - *IBM Corp., Yorktown Heights, NY*

7.8 Solving the SAT Problem Using Noise-Based Logic on FPGAs
Aditya Belsare, Amr Elshennawy, **Sunil Khatri** - *Texas A&M Univ., College Station, TX*

7.9 FPGA LUT Design for Wide-Band Dynamic Voltage and Frequency Scaled Operation
Monther Abusultan, **Sunil Khatri** - *Texas A&M Univ., College Station, TX*

7.10 From RTL Drop to APR in one Day
Victoria Kolesov, Nilesh Karnik, Hoang-Frank Doan, Patrick Nguyen, Tapan Ganpule - *Intel Corp., Folsom, CA*

7.11 Power Regression Methodology Reduces Dynamic Power by 20 Percent
Steven Kommrusch - *Advanced Micro Devices, Inc., Sunnyvale, CA*

7.12 DC to Daylight and Back (On one Ticket)
Nikhil Kriplani - *National Instruments Corp., Austin, TX*
Albert Santos - *AWR Corp., El Segundo, CA*
Joel Dixon, Takao Inoue, Joel Sumner - *National Instruments Corp., Austin, TX*
Joe Pekarek - *Applied Wave Research, Inc., El Segundo, CA*

7.13 Die-Level, Fine-Grain Thermal Analysis Incorporating Package Effects
Vishak Venkatraman, **Srini Krishnamoorthy**, Thomas Burd - *Advanced Micro Devices, Inc., Sunnyvale, CA*

7.14 Hybrid Prototyping of Tightly-Coupled Processor Arrays for MPSoC Designs
Frank Hannig - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*,
Srinivas Boppu, Frank Hannig, Jürgen Teich - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*
Troy Scott - *Synopsys, Inc., Hillsboro, OR*

7.15 Macro-Level ESD Dynamic Simulation and Critical Path Tracing of CDM Events
Ting Ku, Jau-Wen Chen, Yasir Mirza, George Kokai - *NVIDIA Corp., Santa Clara, CA*
Norman Chang, Bo Hu, Ying-Shiun Li - *Apache Design, Inc. a subsidiary of ANSYS, Inc., San Jose, CA*

7.16 Formal Verification of Timing Constraints and Mode Merging Using Fishtail
Chillara Kiran Kumar - *Texas Instruments India Pvt. Ltd., Bangalore, India*
Venkatraman Ramakrishnan - *Texas Instruments, Inc., Bangalore, India*

7.17 Application of Formal Verification for Dynamic Frequency Scaling with Multiple Clock Domain
Masanori Kurimoto, Hirokazu Yoneda, Masayuki Sato, Kota Sakai, Satoshi Kaneko, Naoto Okumura - *Renesas Electronics Corp., Itami, Japan*

7.18 Accurate Boundary Wire Modeling in Hierarchical Timing
Adil Bhanji - *IBM Server and Technology Group, Hopewell Junction, NY*
Gregory Schaeffer, Debjit Sinha, Alex Rubin, **Ravi Ledalla**, Jeffrey Ritzinger, Christine Casey - *IBM Systems and Technology Group, RESEARCH TRIANGLE PARK, NC*

7.19 Top-Level Wire Synthesis and Design Closure
Zhuo Li, Charles Alpert - *IBM Research - Austin, TX*

7.20 UPF Hierarchy Design Flow: The Recipes to Build Billion Gate, Low-Power SoCs
Jianfeng Liu, Jaehan Jeon, Mi-Suk Hong, Kyung-Tae Do, Hyo-Sig Won, Jung Yun Choi, Kee Sup Kim - *Samsung, Yongin, Republic of Korea*

7.21 An Ecosystem Approach for Efficient and Productive Analog/Mixed-Signal Design
Al Lipinski - *Incentia Design Systems, Inc., Santa Clara, CA*
Jeff Miller - *Tanner EDA, Monrovia, CA*
David Rinehart - *Aldec, Inc., Henderson, NV*
John Zuk - *Tanner EDA, Monrovia, CA*
Dmitry Melnik - *Aldec, Inc., Henderson, NV*

7.22 A Versatile RTL-to-RTL Partitioning Methodology and Tool
Krishnan Sundaresan, **Tom Mitchell**, Quan Tran, Yibin Xia, Mohd Jamil Mohd, Derek Urbaniak - *Oracle Corp., Austin, TX*

7.23 Assertions as Functional Checker: How We Erased the Boundary between Testbench and Assertion Domains
Ashish Deokule, Kunal Mishra, **Swapnajit Mitra** - *PLX Technology Inc., Sunnyvale, CA*

7.24 Clock Methodology for Low-Power Designs and Timing Closure
Deepti Miyan - *STMicroelectronics, Greater Noida India, India*

7.25 Formal - An Integral Part of Chip Design
Normando Montecillo, William Su - *Broadcom Corp., Santa Clara, CA*

7.26 Maximizing Self Gating Efficiency
Ambar Mukherji, Niraj Mehta - *Intel Corp., Bangalore, India*

7.27 Bridging the gap between Latest Methodologies and Older HDLs
Siddhartha Mukherjee - *Truechip Solutions Pvt., Ltd., Noida, India*

POSTER SESSION 2 *(CONTINUED)*

7.28 Method for Non-Simulation Based Estimation of Input pin Capacitance of Hard IPs
Kannan N - *Freescale Semiconductor, Inc., Noida, India*

7.29 Design Strategies Using 2D Toolsets for 3D TSV Chip Stacks Featuring 4096b Wide I/O at 100GB/s
Makoto Nagata, Satoshi Takaya - *Kobe Univ., Kobe, Japan*
Atsushi Sakai, Shiro Uchiyama, Harufumi Kobayashi, Hiroaki Ikeda - *Association of Super-Advanced Electronics Technologies, Tokyo, Japan*

7.30 Performance Improvement of Subversion(r) from the Perspective of Integrated Circuit Design
Radoslav Prahov, Holger Schmidt, Achim Graupner - *ZMDI, Dresden, Germany*

7.31 Layout-Friendly, Automatic Load Splitting While Preserving Existing Layout
Lokesh Nema, Vijay Gupta - *Intel Corp., Bangalore, India*

7.32 On-Die PDN Modeling and Verification for a GDDR5 Interface
Fei Guo - *Advanced Micro Devices, Inc., Markham, ON, Canada*
Chris Ortiz - *Apache Design, Inc. a subsidiary of ANSYS, Inc., San Jose, CA*

7.33 Adopting Formal Methods to Increase Productivity and Quality in the Verification of ARM-Based CPU Subsystems
James Pascoe - *STMicroelectronics, Bristol, United Kingdom*

7.34 Apache Macro Modeling for Power-Grid Analysis on AMD's Jaguar Computer Unit
Aalap Patel, Teja Singh - *Advanced Micro Devices, Inc., Austin, TX*

7.35 Variable Latency VLSI Design Based on Timing Analysis, Delay ATPG, and Completion Prediction
Juan Portillo, Lu Wang, Bao Liu - *Univ. of Texas at San Antonio, TX*

7.36 A Leakage Power Optimization Framework for Full, Custom-Designed Macros Using Multiple-Vt Swapping
Yaping Zhan, David Newmark - *Advanced Micro Devices, Inc., Austin, TX*

7.37 GPHASE: A Clock Checker for Full Custom-Designed Macros in Microprocessors and its Applications in Timing Analysis
Yaping Zhan, David Newmark - *Advanced Micro Devices, Inc., Austin, TX*
Rudy Albachten - *Altera Corp., Austin, TX*

7.38 Turning Failures into Dollars: Results of a Volume Diagnostic Analysis Pilot
Darrell Carder - *Freescale Semiconductor, Inc., Austin, TX*

7.39 FPGA Chip Verification Using UVM
Ravi Ram - *Altera Corp., San Jose, CA*
Charles Zhang - *Paradigm Works, Inc., Andover, MA*
Manish Mahajan - *Altera Corp., San Jose, CA*

7.40 Placement Dependent Variability Assessment of Standard Cell Libraries
Concetta Riccobene, Robert Armstrong, Bob Davis, Kausar Banoo, Rich Laubhan - *LSI Corp., Fort Collins, CO*
Philippe Hurat, Wei Xu, Huiyuan Song - *Cadence Design Systems, Inc., San Jose, CA*

7.41 A Hybrid Clock Tree
Subrata Sen - *Synopsys, Inc., Mountain View, CA*
Steven Yang - *Aquantia Corp., Milpitas, CA*

7.42 Unified Method for Package-Induced Power Supply Droop Analysis
Mahesh Sharma, Ben Beker, Aaron Grenat, Stephen Kosonocky - *Advanced Micro Devices, Inc., Fort Collins, CO*
Chris Ortiz - *Apache Design, Inc. a subsidiary of ANSYS, Inc., San Jose, CA*
Tom Taylor, Jalal Wehbeh - *Advanced Micro Devices, Inc., Austin, TX*

7.43 Automatic Generation of DFM Via Definitions
Puneet Sharma, Chi-Min Yuan - *Freescale Semiconductor, Inc., Austin, TX*

7.44 Formal Verification Applied to the Renesas MCU Design Platform
Toru Shimizu, Satoshi Nakano - *Renesas Electronics Corp., Itami, Japan*
Colin Mason - *OneSpin Solutions GmbH, Tokyo, Japan*

7.45 Statistical Analysis of Diagnosis Data for Efficient Low-Yield Disposition
Andal Jayalakshmi, **Jayaraman Sridhar**, Low Kwang Ming - *Intel Corp., Penang, Malaysia*

7.46 Scalable Hierarchical CDC Verification
Venkataraman Srinivasagam, Venkat Ghanta, Venkat Ghanta, Jaga Shanmugavadivelu - *Cisco Systems, Inc., San Jose, CA*

7.47 Assessing Energy-Speed Trade-Offs for Sub- and Near-Threshold Voltage Scaling in Digital CMOS
Kleber Stangherlin, Sergio Bampi - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

7.48 IR Drop aware GCDN Design
Mahadevan Suryakumar, Prashant Joshi, Sami Kirolos, Peter Wang, Nicholas Tsang - *Intel Corp., Austin, TX*

7.49 Verification Challenges in a Power-Hungry, Smart World
Deepmala Sachan, **Bharathi Venkatesh** - *Intel Corp., Banagalore, India*

7.50 Programmable Virtual Clock Channel Design for SoC
Siong Kiong Teng, Cheong Siak Yeap - *Intel Corp., Halaman Kampung Jawa, Malaysia*

7.51 Pioneering an On-the-Fly Simulation Technique for the Detection of Layout-Dependent Effects During IC Design Phase
Amr Tosson - *Mentor Graphics Corp., Cairo, Egypt*
Rami Salem - *Qualcomm Technologies, Inc., Markham, ON, Canada*
Ahmed Ramadan - *Mentor Graphics Corp., Cairo, Egypt*

7.52 Vantage: An Automated Debug Methodology for Multi-Core Platforms
Vivekananda Vedula - *Freescale Semiconductor, Inc., Austin, TX*

7.53 Power Estimation in Low-Power Microcontrollers and Mixed-Signal Designs
Joseph Yiu - *ARM, Ltd., Cambridge, United Kingdom*
Qi Wang, Pete Hardee - *Cadence Design Systems, Inc., San Jose, CA*

7.54 Unleashing the Power of the Command-Line Interface
Jeremy Webb, Bevan Baas - *Univ. of California, Davis, CA*

7.55 Address Map Automation
Richard Weber, Jamsheed Agahi - *Semifore, Inc., Palo Alto, CA*

7.56 A Study on High Speed Design Margining of Different Topologies of the VCO at 22 nm Technology
Rahul Sharma, Bhawna Tomar, **Anshu Jain** - *Intel Corp., Bangalore, India*

▶1 AUSTIN PROCESSOR HISTORY AND THREE DSPs

Hall 5
Designer Track

Monday, June 3: 11:00am - 1:00pm

DT

Designed in Texas begins with an overview of how Austin ended up with so many designers--by an IBM designer that played a major role. The session continues with talks on DSPs from Qualcomm, Coherent Logix, and Maxim.

Chair:
Raghuram Tupuri - *Advanced Micro Devices, Inc., Austin, TX*

1.1 Collaborations in Austin That Helped Shape the Processor Industry

Jim Kahle has been designing RISC Microprocessors for IBM in Austin since the early '80s. He has led two major collaborations AIM (Apple, IBM, Motorola) and STI (Sony, Toshiba, IBM). Jim will discuss the structure of these collaborations, the influence on the industry, and how these activities helped form a critical mass of designers in Austin.

Jim Kahle - *IBM Corp., Austin, TX*

1.2 Hexagon – Qualcomm's Austin-Designed DSP

We will present an overview of the Hexagon DSP, designed in Austin and used in most current Qualcomm chips. The presentation will include a overview of the DSP architecture, the role of the DSP in Qualcomm products, and consumer technologies enabled by the processor. The presentation will also include a brief history of the DSP design team, how it came to be located in Austin, and what has been accomplished.

Paul Bassett - *Qualcomm Technologies, Inc., Austin, TX*

1.3 Coherent Logix Many-Core DSP Based on HyperX™ Technology

A third generation Austin-designed 100 core DSP chip (hx3100™ processor) in 65nm technology will be described. An overview of the goals, architecture, design challenges, and results (including actual power efficiency) will be presented. A brief view of the programming model will also be given. Finally, market segments of interest will be discussed.

Carl Dobbs - *Coherent Logix, Austin, TX*

1.4 Maxim's TINI Audio Hub – A Fully-Integrated, Portable Audio Solution

Maxim's line of Audio Hubs provide fully integrated audio solutions for the mobile audio market. This talk will focus on the coordination between different disciplines required to combine Maxim's best-in-class analog performance with the DSP horsepower required for the advanced voice and audio algorithms in today's smartphones and tablets. The discussion will include tool flows utilized to develop and introduce customer solutions that aren't merely pieces of silicon, but that also include a significant software component.

Brian Trotter - *Maxim Integrated, Austin, TX*

▶2 PHYSICAL DESIGN I

Hall 5
Designer Track

Tuesday, June 4: 10:30am - 12:00pm

Designers from AMD, Freescale, and Everspin talk about physical design methodologies on CPU cores, SoC power management with biasing, and Magnetoresistive RAM.

Moderator:
Jonathan Dement - *IBM Corp., Austin, TX*

2.1 Physical Design Methodologies on AMD's CPU Cores

This presentation will cover the physical design methodologies and CAD flows used on AMD's low-power (Jaguar) and high-performance (SteamRoller) CPU cores. Both CPU cores used a wide variety of construction techniques including full-custom macros, custom-placed blocks and synthesis/P&R. Each of these methodologies along with corresponding tool flows will be discussed. We will also give an overview of the tools and methodologies used for static timing, IR, electro-migration, power consumption analysis, leakage recovery and clock/voltage domain crossing. The presentation will highlight some of the unique tool flows developed around in-house and industry-standard CAD tools.

Mahesh Sharma - *Advanced Micro Devices, Inc., Austin, TX*

2.2 SoC Power Management Using Biasing Techniques

This presentation summarizes various techniques used on 90nm & 55nm designs to reduce leakage power by 75% on 90nm and 50% on 55nm designs with minimal performance penalty. It will also describe the tool limitations encountered in constructing these SoC's. Some of the additional complexities seen at 40nm and 28nm will be covered inherent in the larger variations of the smaller geometries.

Dave Tipple - *Freescale Semiconductor, Inc., Austin, TX*

2.3 Design, Technology, and Commercialization of Magnetoresistive RAM

Everspin's Magnetoresistive Random Access Memory (MRAM) combines magnetic storage elements with a standard CMOS logic process to obtain the benefits of non-volatility, RAM speed and unlimited read/write endurance, a combination not found in other existing volatile or non-volatile commodity memory technologies. The first generation Toggle MRAM has been widely adopted in storage systems, industrial computing, cognitive computing, automotive, and aerospace application. Everspin recently introduced the second generation Spin-Torque MRAM (ST-MRAM), announcing fully functional 64Mb DDR3 ST-MRAM working samples that offer a new persistent memory solution for non-volatile buffers and caching applications as well as deliver a new nanosecond-class, gigabyte-per-second non-volatile storage tier. This presentation will discuss technology-circuit co-design considering ST-MRAM technology attributes, read and write circuit characteristics, and architecture considerations in MRAM chips.

Syed Alam - *Everspin Technologies, Inc., Austin, TX*

▶3 PHYSICAL DESIGN II

Hall 5
Designer Track

DT

Tuesday, June 4: 1:30 - 3:00pm

Designers from IBM, TI, and Vidatronic will talk about bridging the gap between synthesis and custom design, top-level closure, and low-dropout linear regulators.

Moderator:
Mehmet Yildiz - *Cadence Design Systems, Inc., Austin, TX*

3.1 Structured Soft Blocks: Bridging the gap between Custom and Synthesized Designs

It is well known that today's technology evolution is showing saturation in the area of circuit performance, while the capacity trend line remains healthy. As a result, design teams today are leveraging new technology nodes as a means to integrate larger amounts of function onto chips. As this trend line continues and design content grows, it is becoming increasingly difficult for processor designs to rely exclusively on heavy customization. Productivity methods are in demand, leading processor designs to more highly leverage physical synthesis methods mixed with custom design. Coming from the other end of the spectrum, many ASIC design teams are driving up the stack to higher performance points. These designs can benefit directly from selectively leveraging custom design methods that are more traditionally applied to processor chips. In both cases, there is a trend line driving a mix of custom and synthesized logic. In this talk I will present a design method that sits just at the line that segregates custom and synthesized circuit design. This method is called "structured soft block", or SSB. The SSB method brings the best of both words together into an integrated tools and methodology, allowing some of the key attributes of custom design to be seamlessly merged into the higher productivity physical synthesis method.

Paul Villarubia - *IBM Corp., Austin, TX*

3.2 Rapid Fire – Top Level Closure, Texas Style

Top-level physical design of large complex SoCs can become an unacceptable schedule long pole if using "classic" methodology. Rapid Fire replaces two key classic methodology steps, place_opt & CTS, with a simple, fast, and predictable in-house tool. This tool reduces our closure cycle from weeks to 1 or 2 days, allowing us to run dozens of iterations over the course of a project. Repeatability is improved such that closure cycles can continue until a few weeks prior to base tapeout. We will present the tool, how it fits in the flow, and QOR challenges of top level: flight delay, congestion, power, CTS.

Bob Sussman - *Texas Instruments, Inc., Dallas, TX*

3.3 Low-Dropout (LDO) Linear Regulator: Tutorial and Product Examples

Low-dropout (LDO) linear regulators are an essential component for today's wireless and wired systems. This presentation will discuss background information and requirements for high performance low dropout (LDO) linear regulators both for embedded and discrete applications. The presentation will also discuss performance figures of merit (e.g. power supply rejection and load transient regulation) as well as design trade-offs for different architectures. Finally, the presentation will show some of the LDO products designed at Vidatronic.

Edgar Sanchez-Sinencio - *VIDATRONIC, Inc., College Station, TX*

▶4 DESIGN METHODOLOGIES FROM ESL TO FAULT-TOLERANCE

Hall 5
Designer Track

Tuesday, June 4: 4:00 - 6:00pm

Methodologies for addressing today's complex designs will be presented by designers from LSI, Asset-Intertech, Freescale, and Maxim. These methodologies include transaction-level modeling with SystemC, test and design for test, fault-tolerant architecture, and a mixed-signal methodology.

Moderator:
Ed Nuckolls - *Freescale Semiconductor, Inc., Austin, TX*

4.1 Adding SystemC TLM to a RTL Design Flow

Over recent years the EDA community has embraced the Electronic System Level (ESL) design flow, SystemC, Transaction Level Modeling (TLM) and High Level Synthesis (HLS). Today all major EDA vendors provide the tools needed for an ESL design-flow. With these tools in place design teams need to develop a flow that provides early return on investment, creates an ESL foundation and do this with minimum disruption to active designs and design-flow.

This presentation will explore the most common ESL use-cases and their relation to traditional SoC design flow. Some use-cases focus on single functional blocks, others model major sub-systems, and the virtual system prototype use-case models the complete system. Models of IP blocks are characterized by their functional and performance accuracy and their speed of execution. A model used by a specific use-case will, by necessity, emphasize or de-emphasize these characteristics. Models for a virtual system prototype will emphasize functional accuracy and de-emphasize timing accuracy. Models for performance analysis will emphasize timing accuracy and de-emphasize data and non-performance-critical functionality.An example ESL design-flow identifies the opportunities and challenges as a team's traditional RTL design-flow evolves to an ESL design flow that includes architecture, hardware, design-verification and software.

Bill Bunton - *LSI Corp., Austin, TX*

4.2 Test and Design-for-Test

Al Crouch - *ASSET InterTech, Inc., Austin, TX*

4.3 Design of Fault Tolerant Architecture in System on Chip

This presentation will describe a modified TMR methodology (Triple Module Redundancy) that is suitable for large SoC designs. The techniques achieves Fault Tolerant SoC designs without the prohibitive costs of a full TMR scheme.

Rekha Bangalore - *Freescale Semiconductor, Inc., Austin, TX*

4.4 Mixed-Signal Methodology for First Pass Success - Maxim's InTune Digital Power

We will present an overview of the design methodology used to develop the Maxim InTune Digital Power products in Austin. The presentation will include specification development, RTL design, analog circuit design, modeling, and verification. Emphasis will be on mixed-signal verification and chip build and assembly. The talk will include the first generation product and discuss how the design flow enabled the quick development of the second derivative product. We will also discuss FPGA emulation and how it was used in the development.

Scott Herrington - *Maxim Integrated, Austin, TX*

▶5 FPGAs, APUs, AND AUTOMOTIVE MICROCONTROLLERS

Hall 5
Designer Track

Wednesday, June 5: 9:00 - 10:30am

DT

Designers from Altera, AMD, and Freescale present SoC FPGA's, accelerated processing units, and low-power automotive mircoontrollers.

Moderator:
Shahram Salamian - *Intel Corp., Austin, TX*

5.1 Altera SoC FPGAs

Altera SoC FPGA's monolithically integrate an ARM-based hard processor system (HPS) – which includes CPU's, peripherals, and memory interfaces - into Altera's industry leading 28nm low power FPGA fabric using a high-bandwidth interface. The SoC FPGA combines the performance and power efficiency of hard intellectual property (IP) with the flexibility of programmable logic, while enabling our customers to take advantage of the large and growing ARM software eco-system.

Altera opened the Austin Technology Center (ATC) in 2011 in order to add SoC expertise to the traditionally full custom FPGA company. The ATC team led the effort to successfully bring the SoC FPGA to silicon. This talk will cover the design methodologies used, and some of the unique challenges encountered in integrating an SoC into an FPGA.

Kevin Broe - *Altera Corp., Austin, TX*

5.2 AMD APUs: Dynamic Power Management Techniques

This presentation discusses AMD's "Richland" APU for desktop and notebook applications. Topics will include overall APU architecture as well as a discussion of CPU and graphics cores, multimedia, memory, interconnect and I/O and the design flow used to bring it all together. A discussion of dynamic power and performance management mechanisms will be included as well.

Praveen Dongara - *Advanced Micro Devices, Inc., Austin, TX*

5.3 Low-Power Design Techniques for Automotive Microcontrollers

Automotive environments can present harsh conditions for Multi-Core MCUs. This is especially true for power management. With operating temperature above 165C and Always On computing, power reduction can be very challenging. The presentation will discuss system, logic and adaptive circuit techniques used for achieving aggressive power budgets.

Anis Jarrar - *Freescale Semiconductor, Inc., Austin, TX*

▶6 HIGH-PERFORMANCE PROCESSORS AND SOCs

Hall 5
Designer Track

Wednesday, June 5: 4:00 - 6:00pm

Designed in Texas concludes with speakers from IBM, ARM, Intel, and Samsung presenting challenges encountered during recent flagship processor and SoC designs.

Chair:
Sumit DasGupta - *Silicon Integration Initiative, Inc., Austin, TX*

6.1 On Constructing the IBM Power 7+ Microprocessor

The IBM Power 7+ is a XXGHz, eight-core microprocessor designed using IBM's 32nm SOI process. This paper gives an overview of the P7+ and describes the techniques and methodologies utilized in its implementation.

Jose Paredes - *IBM Corp., Austin, TX*

6.2 High Performance, Energy Efficient ARM Cortex Processors and CoreLink Interconnect Technology

Austin is an important design center for ARM, producing some of the key processor and interconnect technology ARM offers for enterprise and mobile applications. Some of the recent products designed in Austin that are the subject of this talk include the ARM® Cortex®-A15 multi-core processor, the Cortex-A57 multi-core processor, and the CoreLink™ CCN-504 cache coherent interconnect. The development of each of these products required an experienced team of designers experienced in RTL, verification, validation, and implementation, as well as coordination and collaboration with other ARM design sites. This talk briefly describes the innovation behind these products and the markets they serve. Finally, we look at the vital role the Austin-based engineering team played, contributing to the development and delivery of these technologies.

Mike Filippo - *ARM, Inc., Austin, TX*

6.3 Designing High-Performance Intel® Atom™ SoCs

We will present the design of complex Intel® Atom™ SoCs targeted for high-performance smartphones. We will begin by discussing key differentiators required for the high-end smartphone segment. We will overview design challenges that we have encountered and solutions that involve design methodology, flows, and tools. We will also provide a brief overview of Intel's Austin Design Center.

After discussing the key differentiators of this SoC to win in the high end smartphone segment, we will go over the key architectural features, performance metrics, design challenges and the overall execution from the Austin design center in Texas.

Mourad Aberbour - *Intel Corp., Austin, TX*

6.4 Designing a Processor for Advanced Mobile Devices

Aaron Lindner - *Samsung, Austin, TX*

DAC MANAGEMENT DAY 2013

Room: 17AB
General Interest

MD

Today's complex SOCs require different types of optimizations and the adoption of emerging solutions to meet such requirements. Optimizing for volume production, low power, and shrinking sizes necessitates accurate trade-off analysis and technical/business decision-making by management. Also, moving to new semiconductor technology nodes, such as 16nm or 20nm, can significantly affect the choices of suppliers. The Management Day sessions will discuss these changing needs and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options for flows, methodologies, and suppliers.

The Management Day is comprised of two sessions, which will feature presentations by managers representing fabless and fablite companies, systems houses and suppliers to the design ecosystem. Senior managers will discuss the latest and emerging solutions, along with their economic impact.

Organizer:
Yervant Zorian - *Synopsys, Inc., Mountain View, CA*

SESSION 1: TRADE-OFFS AND CHOICE FOR EMERGING SOCS
10:30am - 12:00pm

Today's emerging SOC industry requires multiple types of optimization to adopt advanced solutions that meet stringent design requirements. Optimizing for volume production, low power, and shrinking sizes in globally distributed companies necessitate adequate trade-off analysis and technical/business decision-making by management. This session will feature senior managers from our ecosystem who will share their experiences.

Presenters:
Pike Powers – *Partner, Fulbright & Jaworski LLP, Austin, TX*
Ron Martino – *Vice President Automotive R&D, Freescale, Austin, TX*
Andrew Chang – *Corporate Vice President, MediaTek, Hsinchu City, Taiwan*

SESSION 2: DECISION MAKING FOR COMPLEX ICS
2:00 - 4:30pm

Moving to new semiconductor technology nodes for complex ICs can significantly affect the choices of design flow, methodologies and suppliers. This session will cover the challenges of complex chip design and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options. This session feature presentations by senior managers representing a range of today's most complex nanometer IC design suppliers

Presenters:
Kee Sup Kim – *Vice President, Design Technology, Samsung Electronics, Yongin City, Korea*
J.C. Parker – *Engineering Director Design Tools & Methodology, LSI, Allentown, PA*
Rex Berridge – *Microprocessor Design & Automation Manager, IBM, Austin, TX*
Bob Madge – *Director Design Enabled Manufacturing, GLOBALFOUNDRIES, Milpitas, CA*

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The 50th DAC has introduced a new category in the technical program -- SKY Talks. SKY is an abbreviation for Short KeYnotes, each 30 minutes long. There are two SKY talks each afternoon on Tuesday, Wednesday, and Thursday. The collection of SKY talks for 2013 cover a wide variety of topics with broad appeal to the DAC audience, with an overall focus on the needs and trends of our industry.

▶13 POST-EXPONENTIAL INNOVATION

Room: 16AB
General Interest

Tuesday, June 4 - 2:30 - 3:00pm

ST

As the microprocessor and system performance exponential slows other aspects of system design are moving to the forefront. While there are many new design optimization's being explored by the industry such as special purpose accelerators, appliance like optimization of general purpose systems, and exploitation of new system technologies such as flash, this talk will focus these and other optimizations. The post performance exponential era is also ushering in the rise of new IT consumption models that are having a huge impact on the way systems are designed as well as delivered to customers. These impacts will be described as well and discussed with an eye towards design impacts.

Moderator:
Charles Alpert - *IBM Corp., Austin, TX*

Presenter:
Brad McCredie - *IBM Corp., Austin, TX*

▶20 WHAT A CHIP DESIGNER NEEDS AT THE END OF MOORE'S LAW

Room: 16AB
Analog/Mixed-Signal/RF Design

Tuesday, June 4 - 5:30 - 6:00pm

If a non-technical person looks around and sees the incredible array of highly complex, high capable silicon in the world today, they might reasonably conclude that most aspects of chip design have been mastered. After all, it's now been 20 years since the Pentium FDIV flaw. But chip engineers know better - there are aspects of chip design that have never been fully conquered, and some of them are about to get much worse. In this talk I'll explore what a chip designer of the relatively near future is going to need, to continue (at least for a few more years) the illusion that routine creation of these chips can be taken for granted.

Moderator:
Robert Jones - *Intel Corp., Hillsboro, OR*

Presenter:
Robert Colwell - *Defense Advanced Research Projects Agency, Arlington, VA*

▶33 21ST CENTURY DIGITAL DESIGN TOOLS

Room: 16AB
General Interest

Wednesday, June 5 - 2:30 - 3:00pm

Most chips today are designed with 20th century CAD tools. These tools, and the abstractions they are based on, were originally designed to handle designs of one million gates or less. They are not up to the task of handling today's billion gate designs. The result is months of delay and considerable labor from final RTL to tapeout. Surprises in timing closure and power consumption are common. Even taking an existing design to a new process node is a time-consuming and laborious process.

21st century CAD tools should be based on higher-level abstractions to enable billion gate chips to go from final RTL to tapeout in days, not months. Key to attaining this increase in productivity is raising the level of design and using simple, standard interfaces. Designs should be composed from high-level modules - processors, modems, codecs, memory subsystems, and I/O subsystems - rather than gates and flip-flops. Each module, which we expect to contain 105 gates or more, is placed as a unit, and communicates over a standard NoC. Restricting modules to standard sizes and aspect ratios further simplifies physical design. We expect even a large chip to contain at most a few thousand such modules and expect the physical design of such a chip to take a few days with minimal labor (after the modules are complete).

Moderator:
Soha Hassoun - *Tufts Univ., Medford, MA*

33.1 Digital Design Tools for the 21st Century
William Dally - *NVIDIA Corp., Stanford Univ., Santa Clara, CA*
Chris Malachowsky - *NVIDIA Corp., Santa Clara, CA*
Stephen Keckler - *NVIDIA Corp., Univ. of Texas at Austin, Santa Clara, CA*

▶40 THE ROLE OF CASCADE, A CYCLE-BASED SIMULATION INFRASTRUCTURE, IN DESIGNING THE ANTON SPECIAL-PURPOSE SUPERCOMPUTERS

Room: 16AB
Verification and Simulation

ST

Wednesday, June 5 - 5:30 - 6:00pm

Cascade is a cycle-based C++ simulation infrastructure used in the design and verification of two successive versions of Anton, a special-purpose machine for molecular dynamics computation. Cascade was engineered to address the size and speed challenges inherent in simulating massively parallel special-purpose machines. The Cascade-based Anton simulators were instrumental for architectural exploration and validation, performance estimation, hardware/software co-design, design verification, and software development.

Moderator:
Donatella Sciuto - *Politecnico di Milano, Milan, Italy*

40.1 The Role of Cascade, a Cycle-Based Simulation Infrastructure, in Designing the Anton Special-Purpose Supercomputers
J.P. Grossman, Brian Towles, Joseph Bank -
D. E. Shaw Research, New York, NY
David Shaw - *D.E. Shaw Research, Columbia Univ., New York, NY*

▶53 SOLVING ANALOG CHALLENGES TO ENABLE THE FUTURE OF ELECTRONICS

Room: 16AB
Analog/Mixed-Signal/RF Design

Thursday, June 6 - 2:30 - 3:00pm

Exciting capabilities are on the horizon as the Internet of Things continues to grow, especially in areas like cloud computing, medical electronics, safety and security and more. Analog technology plays a crucial role in advancing these applications. But for future capabilities to become a reality there are several analog design challenges that must be overcome. This talk will present the trends, challenges and offer solutions, including increased analog integration, the use of new materials, and techniques to reduce leakage, improve power efficiency and performance. Important considerations as the lines between digital and analog continue to blur will also be discussed.

Moderator:
Michael "Mac" McNamara - *Adapt-IP, Palo Alto, CA*
Presenter:
Ahmad Bahai - *Texas Instruments, Inc., Austin, TX*

▶60 ON THE CONVERGENCE OF HIGH-PERFORMANCE AND MISSION CRITICAL MARKETS

Room: 16AB
Embedded Architecture & Platforms

Thursday, June 6 - 5:00 - 5:30pm

The computing market has been dominated during the last two decades by the well-known convergence of the high-performance computing market and the mobile market. In this paper we witness a new type of convergence between the mission-critical market (such as avionic or automotive) and the mainstream consumer electronics market. Such convergence is fueled by the common needs of both markets for more reliability,support for mission-critical functionalities and the challenge of harnessing the unsustainable increases in safety margins to guarantee either correctness or timing. In this position paper,we present a description of this new convergence, as well as the main challenges and opportunities that it brings to computing industry.

Moderator:
Norbert Wehn - *Univ. of Kaiserslautern, Kaiserslautern, Germany*

60.1 On the Convergence of Mainstream and Mission-Critical Markets
Sylvain Girbal - *Thales Group, Palaiseau, France*
Miquel Moreto - *Barcelona Supercomputing Ctr., Berkeley, CA*
Arnaud Grasset - *Thales Group, Palaiseau, France*
Jaume Abella, Eduardo Quinones, Eduardo Quinones -
Barcelona Supercomputing Ctr., Barcelona, Spain
Francisco Cazorla -
Barcelona Supercomputing Center and IIIA-CSIC, Barcelona, Spain
Sami Yehia - *Intel Corp., Hillsboro, CA*

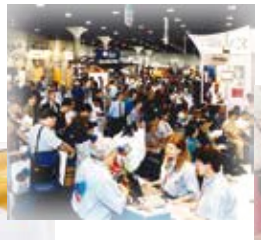
50 YEARS OF
INNOVATION

DESIGN AUTOMATION CONFERENCE



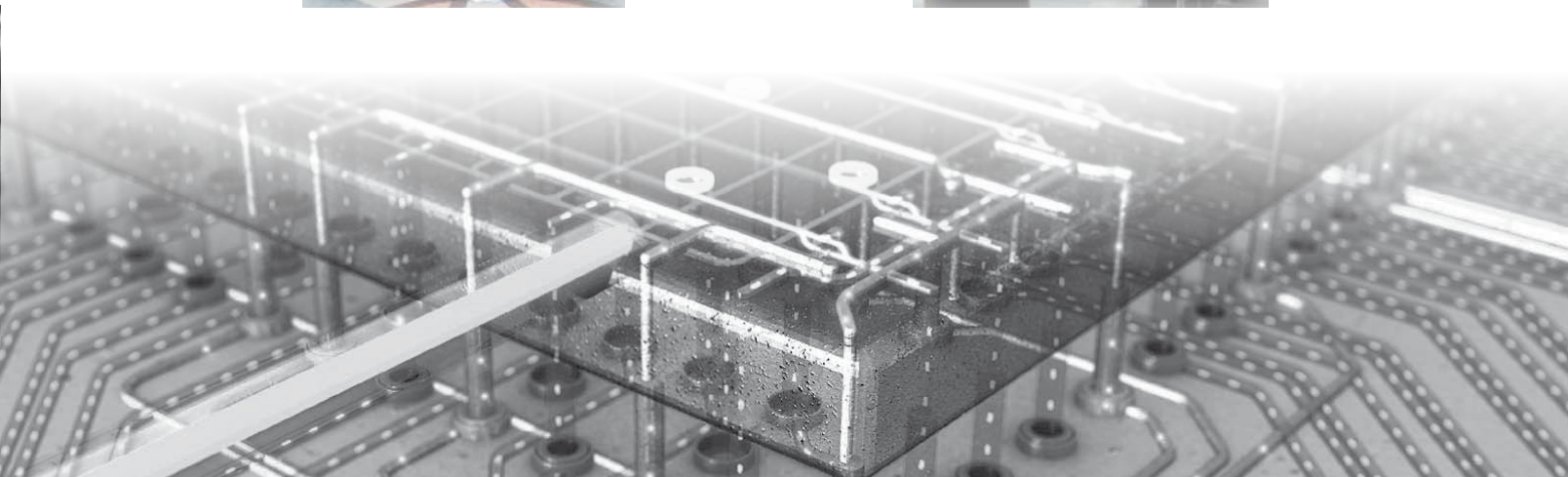






DESIGN AUTOMATION CONFERENCE

50 YEARS OF INNOVATION



▶1 THEY ARE ALL NETWORKS! ANALYSIS AND OPTIMIZATION FOR ELECTRONICS, WATER, ELECTRICITY, BIO. A DAC ASSOCIATED WORKSHOP

Room: 13AB
General Interest

8:30am - 3:00pm

WS

This workshop focuses on the network aspect of problems in different domains as it occurs in water systems, the electricity grid, and biological networks of neurons. As the VLSI electronic systems consist of networks made of transistors, the utility power grids and water distribution pipelines are also large-scale man-made networks. Furthermore, neuron networks inside brains and the networks formed by river channels and lakes are good examples of complex networks in nature. Similar to the transistor circuits, efficient analysis and optimization of large-scale networks in those domains pose significant challenges.

The speakers of this workshop are domain experts both inside and outside of IC industry. They will address the numerous similarities, e.g., solving large systems of differential equations efficiently, topology optimization, uncertainty in models and parameters, but also the substantial differences, such as the emphasis on the operational aspect and situational awareness in case of the power grid and the water system. One presentation will describe the use of 'agent-based' simulation, where the electricity grid is modeled within a complex environment of operators, generators, and customers all interacting through a market mechanism.

Another presentation will describe the efficient simulation of millions of networked neurons using realistic Hodgkin-Huxley models. Real time parameter estimation will be addressed both in the context of water and electricity networks. Here, approximate or empiric models are augmented with real time measurements to provide enhanced situational awareness. The audience will also be exposed to the fundamentals of fluid dynamics and the related simulation challenges.

Organizers:
Peter Feldmann - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Frank Liu - *IBM Research - Austin, TX*

Speakers:
Ben R. Hodges - *Univ. of Texas at Austin, TX*
Frank Liu - *IBM Research - Austin, TX*
Peng Li - *Texas A&M Univ., College Station, TX*
Jason C. Fuller - *Pacific Northwest National Laboratory, Richland, WA*
Peter Feldmann - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

▶2 DAC WORKSHOP ON MODELING OF BIOLOGICAL SYSTEMS (MoBs)

Room: 14
Other

9:00am - 6:30pm

The First Workshop on Modeling of Biological Systems (MoBS) focuses on computational methods and software tools for the modeling and analysis of biological systems. It will bring together researchers from computational systems biology and design automation communities. The field of electronic design automation (EDA) has developed sophisticated methods for optimizing and designing the most complicated machines in the world. The success of EDA is apparent in ubiquitousness of high-performance VLSI systems in every walk of life.

Most, if not all of these systems have been built using one or more tools developed by the EDA community. The computational methods that have been developed to design and analyze such complicated systems can be harnessed in modeling and analyzing biological systems. EDA researchers are highly trained in algorithm development and system design. They possess expertise in a wide variety of computational methods such as convex optimization, automated verification, theorem proving, pattern recognition/clustering and probabilistic or stochastic system modeling, and their viewpoints could bring new results in biology.

We hope to create an environment rich in cross fertilization where different types of researchers interact and start fruitful collaborations. For biologists, this workshop is an opportunity to showcase their work to an entirely new audience and gain exposure to a new talent pool of potential postdocs and graduate students. For EDA experts, this workshop provides an excellent opportunity to explore challenges in biology and medical research, and recognize potential for new collaborations and novel applications of methods and techniques they are familiar with.

Topics of interest at the MoBS workshop include biological network inference, CAD and visualization of biological systems, data-mining for bio and health-care systems, hybrid methods for bio-system simulation, bio-model validation and verification, sensitivity analysis for biological systems and much more.

Organizers:
Subarna Sinha - *Stanford Univ., Stanford, CA*
Natasa Miskov-Zivanov - *Carnegie Mellon Univ., Pittsburgh, PA*
Smita Krishnaswamy - *Columbia Univ., New York, NY*

Speakers:
Edward Dougherty - *Texas A&M Univ., College Station, TX*
Dana Pe'er - *Columbia Univ., Columbia, NY*
Josh Stuart - *Univ. of California, Santa Cruz, CA*
Shuichi Takayama - *Univ. of Michigan, Ann Arbor, MI*

▶3 2013 DAC WORKSHOP ON EMBEDDED SYSTEMS FOR ENERGY-EFFICIENT SMART INFRASTRUCTURES (ESSI)

Room: 18D
Embedded Architecture & Platforms

9:00am - 5:00pm

Smart infrastructures that provide energy-efficient, reliable and secure services are currently hot topics under discussion by government, the media, and the researchers. They can be found in many different applications at different scales, such smart wireless networks, smart meters for smart homes, and smart data centers.

While significantly different in contexts, those applications share one thing in common: they need embedded systems to optimize the performance based on the information/data gathered from the meters/sensors. Depending on the level of smartness, those embedded systems can use the gathered information/data to help improve future designs, or to assist operators to with decision making, or to automatically adjust operations. While smart infrastructures can serve for many purposes, this workshop is particularly interested in those with energy efficiency as the primary target.

Of course, various other factors such as reliability, security, privacy, flexibility and controllability should also be considered. Those metrics together impose stringent constraints on the embedded systems that operate the smart infrastructures. Particular challenges include, but not limited to, the information/data collection without triggering privacy and security issues, the efficient data fusion and analysis, the real-time response design, the robustness in the presence of contingencies, and software/hardware co-design.

A good example of embedded systems in the context of energy-efficient smart infrastructures, which also serve as a sample of the workshop scope, is the smart home. In smart homes, all components such as various household appliances and plug-in hybrid electric vehicles (PHEVs) are connected to home area networks and smart meters, and are controlled through demand side management (DSM) technologies.

With the emerging real-time pricing schemes, DSM can achieve efficient energy usage as well as monetary expense reduction. It also enables the integration of renewable energy resources, and facilitates the peak-to-average load ratio reduction for balancing energy consumption in the power transmission and distribution system. The core of DSM lies in the salient design of appropriate embedded systems to schedule and control the operation of household appliances and PHEVs. Moreover, advanced embedded system optimization techniques can also be explored for more intelligent control.

On the other hand, since smart meters are networked, hackers could remotely tamper smart meter readings or intercept wireless communications from individual smart meters to find the right time for home burglaries. Furthermore, the contingency due to equipment failure and power outage/blackout in the local power distribution network can also significantly impact the performance of the system. Thus, the smart home embedded system designs, which can conserve energy and reduce carbon footprint while considering cyber security and reliability of the system, are highly desired.

Organizers:
Yiyu Shi - *Missouri Univ. of Science and Technology, Rolla, MO*
Shiyan Hu - *Michigan Technological Univ., Houghton, MI*

Speakers:
Marija Ilic - *Carnegie Mellon Univ., Pittsburgh, PA*
Alfonso Valdes - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
David B. Bartlett - *IBM Corp., Yorktown, NY*
Charlie Catlett - *Argonne National Lab, Lemont, IL*
Stephen Boyd - *Stanford Univ., Stanford, CA*
Amy Wang - *Tsinghua Univ., Beijing, China*
Edmund Widl - *Austrian Institute of Technology, Vienna, Austria*
Aiwu Shi - *China Standard Software Company, LTD, Beijing, China*

▶4 DAC WORKSHOP: LOW-POWER DESIGN WITH THE NEW IEEE 1801-2013 STANDARD

Room: 18C
Low-Power Design and Power Analysis

1:00 - 5:00pm

The latest version of the IEEE Std P1801 (Standard for Design and Verification of Low Power Integrated Circuits) was ratified by IEEE-SA on 6th March 2013. The new standard will be known as IEEE 1801-2013. The presenters are all members of the IEEE 1801 working group, and are technical experts on the subject.

The workshop will cover an introduction to the low power design intent concepts and methodologies fundamental to IEEE 1801, as well as detailed discussion of the main changes from the previous version (IEEE 1801-2009). The workshop will concentrate on the standard, its underlying semantics and intended methodologies, in the eyes of the expert 1801 working group members, illustrated by real world examples. Showcasing capabilities of EDA vendor tools is not the focus of this workshop.

Organizer:
Pete Hardee - *Cadence Design Systems, Inc., San Jose, CA*

Speakers:
Qi Wang - *Cadence Design Systems, Inc., San Jose, CA*
Erich Marschner - *Mentor Graphics Corp., Ellicott City, MD*
Sushma Honnavara-Prasad - *Broadcom Corp., Santa Clara, CA*
John Biggs - *ARM, Inc., Cambridge, United Kingdom*
Jeffrey Lee - *Synopsys, Inc., Mountain View, CA*

▶5 DAC WORKSHOP ON COMPUTING IN HETEROGENEOUS, AUTONOMOUS 'N' GOAL-ORIENTED ENVIRONMENTS

Room: 12AB
General Interest

2:00 - 6:00pm

This workshop will present contribution both from companies and universities that are working towards the definition of self-aware and adaptive technologies. We will have the chance to have contributions from pure research prospective while investigating cutting-edge solutions used by companies to designed better systems.

The objective of the event is to bring together researchers and industry from all over the world for a wide ranging discussion on self-aware adaptive systems. Heterogeneous, adaptable multicore systems is one of the main established trends in modern computing architectures. As silicon resources get increasingly abundant, runtime reconfigurable elements can ever more be combined together with heterogeneous processing elements and many cores on a chip by processor designers. Such architectures provide important improvements in system performance, but also pose new research questions to be answered, e.g., will current processor interconnection mechanisms scale to thousands of cores?

Since the conditions influencing runtime behavior cannot be fully known at design time, how is it possible to obtain a system implementation that aims at obtaining the highest possible performance given the underlying hardware architecture? The Self-Aware computing research leverages the new balance of resources to improve performance, utilization, reliability and programmability.

Organizers:
Marco Santambrogio - *Politecnico di Milano, Milan, Italy*
Hank Hoffmann - *University of Chicago, Chicago, IL*

Speakers:
Vijay Janapa Reddi - *Univ. of Texas at Austin, TX*
Simone Campanoni - *Harvard Univ., Cambridge, MA*
Hank Hoffmann - *University of Chicago, Chicago, IL*
Ayse Kivilcim Coskun - *Boston Univ., Boston, MA*
Jan Rellermeyer - *IBM Research - Austin, TX*
Fillippo Sironi - *Politecnico di Milano, Milan, Italy*
Iuliana Bacivarov - *Eidgenössische Technische Hochschule Zürich, Zurich, Switzerland*

▶6 IP WORKSHOP: DRIVING QUALITY TO THE DESKTOP OF THE DAC ENGINEER

Room: 11AB
Designer Track

1:00 - 5:00pm

This workshop will demonstrate a complete flow, using de facto industry standards, for designing, packaging, and integrating semiconductor IP, insuring that quality metrics are observed and preserved throughout the flow to the DAC engineer's desktop. A variety of leading companies will be part of the workshop, each presenting how their individual products work together in a cohesive fashion for the benefit of the SoC designer.

The companies and their contributions to the workshop are as follows:

TSMC will discuss the TSMC 9000™ quality standards and explain how they are beneficial for both IP providers and IP consumers.

Atrenta will demonstrate the use of SpyGlass® and its IP Kit™ for the analysis of IP against a set of standard quality metrics.

Sonics will demonstrate the creation of configurable IP and the manner in which it is validated and checked against quality metrics using the TSMC Soft IP Kit 2.0 flow.

IPextreme will demonstrate the use of Xena™ for storing and managing completed IP products and will also showcase how users can configure IP on-the-fly and re-verify the quality metrics produced from SpyGlass® in the Cloud.

The IP Workshop will realistically showcase how engineers from different companies use their proprietary tools and technology to work together. The result of this collaboration is the creation of high quality, first-time-correct products. Because the flow delves into a number of areas in the design and use of semiconductor IP, the workshop's appeal and relevance is wide. There will be ample time provided for open discussion throughout the workshop—audience members are encouraged to ask questions and share their thoughts and impressions at each stage of the flow. The workshop will conclude with a roundtable session with the presenters.

Organizer:
McKenzie Mortensen - *IPextreme, Campbell, CA*

Speakers:
Warren Savage - *IPextreme, Campbell, CA*
Dan Kochpatcharin - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*
Mike Gianfagna - *Atrenta Inc., San Jose, CA*
Frank Ferro - *Sonics, Inc., Milpitas, CA*
Michael Cizi - *IPextreme, Unterföhring, Germany*
Richard Zbranak - *Atrenta Inc., Austin, TX*
Sveta Avagyan - *Sonics, Inc., Milpitas, CA*
John Bainbridge - *Sonics, Inc., Milpitas, CA*

▶1 MODELING, ABSTRACTION, AND VERIFICATION OF NON-VOLATILE MEMORIES

Room: 11AB
Verification and Simulation

Non-volatile memories (e.g., Flash, MRAM, FeRAM, etc.) are pervasive in embedded systems, including iPods, cellular telephones, medical instruments, automobiles, etc. Memories take up more than 50% of a modern SoC design, both in real estate and transistor count. Consequently, memory verification is a critical component of the verification flow of a modern SoC design. However, traditional techniques for memory verification are inapplicable to non-volatile memories.

This tutorial provides a broad overview of formal functional verification of non-volatile memories. We discuss the traditional approach, its inadequacies, and recent verification techniques crafted to overcome these inadequacies.

This tutorial caters to (1) formal verification engineers interested in nderstanding applicability of the techniques in this domain, (2) memory designers and validators interested in understanding the role of formal analysis for design correctness, and (3) technical managers seeking an understanding of the complexity involoved and techniques employed.

Organizers:
Sandip Ray - *Intel Corp., Hillsboro, OR*
Jay Bhadra - *Freescale Semiconductor, Inc., Austin, TX*

Speakers:
Sandip Ray - *Intel Corp., Hillsboro, OR*
Jay Bhadra - *Freescale Semiconductor, Inc., Austin, TX*

TUT

▶2 METHODOLOGY FOR CONTINUOUS 24X7 VERIFICATION AND COVERAGE

Room: 12AB
Verification and Simulation

The concept of continuous verification is the notion of ensuring that your verification engines, most normally your simulators, are always running and always executing jobs. The "always on" philosophy means that jobs are submitted to the simulation farm on a 24x7 basis, and that no engine is ever sitting idle.

One of the key technical enablers to this "always on" methodology, however, is a significant shift in coverage methodology. Specifically, coverage needs to support the notions of continuous data updates without having to worry so much about model changes. This may require putting more effort in the front end of the process (model definition), but it provides more capabilities at analysis time. The tutorial describes in detail the coverage aspects of the continuous verification methodology, discusses the challenges and benefits this approach provides, and explains how users might apply a similar approach in their own projects.

Organizers:
Avi Ziv - *IBM Corp., Haifa, Israel*
John Brennan - *Cadence Design Systems, Inc., Chelmsford, MA*

Speakers:
Avi Ziv - *IBM Corp., Haifa, Israel*
Hemant Gupta - *Cadence Design Systems, Inc., Noida, India*

▶3 WINNING IN MONTE CARLO: MANAGING SIMULATIONS UNDER VARIABILITY AND RELIABILITY

Room: 13AB
Design for Manufacturability

Thanks to FinFETs and other process innovations, we are still shrinking devices. But it comes at a steep price: variability and reliability have become far worse, so effective design and verification is causing an explosion in simulations. First, Daniel Nenni will do the introductions and present process variation content and analytics from SemiWiki.com. Presenter Prof. Georges Gielen, will describe CAD and circuit techniques for variability and reliability.

Next, Yu (Kevin) Cao from ASU will describe how variability and aging affect bulk vs. FinFET device performance. More corners and statistical spreads will come into play, so advanced IC design tools will be needed to minimize design cycle times. Then, Trent McConaghy from Solido Design Automation, will describe industrial techniques for fast PVT, 3-sigma, and high-sigma verification. Finally, Ting Ku, Director of Engineering at Nvidia, will describe a signal integrity case study using variation-aware design techniques.

To Monte Carlo... and beyond!

Organizers:
Trent McConaghy - *Solido Design Automation, Inc., Vancouver, BC, Canada*
Georges Gielen - *Katholieke Univ. Leuven, Belgium*

Speakers:
Daniel Nenni - *SemiWiki, Danville, CA*
Georges Gielen - *Katholieke Univ. Leuven, Belgium*
Yu (Kevin) Cao - *Arizona State Univ., Tempe, AZ*
Trent McConaghy - *Solido Design Automation, Inc., Vancouver, BC, Canada*
Ting Ku - *NVIDIA Corp., San Jose, CA*

▶4 A PRACTICAL GUIDE TO PACKAGING IP AND ASSEMBLING SOCS USING THE IP-XACT- IEEE1685 STANDARD

Room: 14
System Level Design and Communication

This tutorial will appeal to those new to the IP-XACT- IEEE1685 standard as well providing additional insight into more advanced IP-XACT topics. The tutorial will be presented by IP-XACT experts and will begin with an introduction to the fundamental concepts of IP-XACT, followed by a series of 'how-to' topics. Attendees will initially be brought through IP Packaging topics such as creation of bus definitions, bus interfaces and HW/SW interface representation. Integration topics will focus on representing hierarchical designs through instantiating components and connectivity.

The 2nd half of this tutorial will focus on more advanced topics including generators, SCR compliancy checks, channels, bridges, parameters and design configurations. The presentation technique will focus more on visually presenting the IP-XACT concepts rather than walking through XML snippets.

TUT

Organizers:
David Murray - *Duolog Technologies Ltd., Galway, Ireland*
Kathy Werner - *Southwest Reuse, Austin, TX*

Speakers:
David Murray - *Duolog Technologies Ltd., Galway, Ireland*
John Eaton - *Ouabache Designworks, Vancouver, WA*
Vasant Kumar Easwaran - *Texas Instruments India Pvt. Ltd., Bengaluru, India*
Mark Noll - *Synopsys, Inc., Portland, OR*
Kamlesh Kumar Pathak - *STMicroelectronics, Greater Noida, India*
Sylvain Duvilliard - *Magillem Design Services, Cannes, France*

▶5 SUPERCHARGE YOUR GPU: DEVELOPING AND OPTIMIZING OPENGL APPLICATIONS USING A NATIVE IDE ACROSS VIRTUAL AND PHYSICAL TARGETS

Room: 15
General Interest

OpenGL ES is an Application Programming Interface (API) specification for 3D computer graphics programming that offers 3D geometric object generation, image manipulation and high-quality scene rendering.

In this tutorial, we will present the evolution of an OpenGL ES application development and execution flow across software and hardware threads and through virtual and physical embedded hardware targets. The entire flow is driven with a unified native Software IDE with embedded hardware visibility and profiling features.

The tutorial will delve into all aspects of software-driven debugging and optimization while migrating from a pure virtual prototype target, and software rendering implementation across to graphical processing engine executing on an emulator or a physical board.

The real-world impact of the flow described in this tutorial is far reaching. Graphical applications such as visual computing, image processing and 3D animation and navigation are a fundamental component of many modern mobile, automotive and gaming devices.

Organizers:
Carole Dunn - *Mentor Graphics Corp., Wilsonville, OR*
Rami Rachamim - *Mentor Graphics Corp., Herzilya, Israel*

Speakers:
Jon McDonald - *Mentor Graphics Corp., Wilsonville, OR*
Mark Bellamy - *ARM, Inc., Austin, TX*

▶6 WHY PROGRAMMING MANY-CORE IS NOT MISSION IMPOSSIBLE

Room: 16AB
Embedded Software

Attendees will learn how a many-core processor can be programmed using C and the industry standard Message Passing Interface "MPI". A DSP processor based on HyperX™ technology will be used as the demonstration vehicle. A structured approach to system analysis will be described that produces an optimal mapping of an algorithm to processing resources.

An example will be used to show in-depth analysis and subsequent mapping to processing resources. Additionally, a full LTE PHY and an H.264 encoder will be demonstrated. Throughout the tutorial, an interactive Eclipse-based environment is used for development and running the resulting programs on a cycle-accurate instruction set simulator and target hardware.

The intended audience for this tutorial is algorithm developers of embedded systems. Knowledge of C programming is required. Familiarity with basic DSP principles will be helpful. Concepts covered will include parallel programming methods, structured system and algorithm analysis, and embedded system development and debug.

Organizer:
Michael Solka - *Coherent Logix, Austin, TX*

Speakers:
Bryan Schleck - *Coherent Logix, Austin, TX*
MK Sandeep - *Coherent Logix, Austin, TX*

▶7 AVOIDING CORE MELTDOWN! - ADAPTIVE TECHNIQUES FOR POWER AND THERMAL MANAGEMENT OF MULTI-CORE PROCESSORS

Room: 18C
Low-Power Design and Power Analysis

The objective of this embedded tutorial is to bring DAC attendees who are interested in low-power design for high-end, multi-core processors to the forefront of the latest academic research and industrial practice in the area of closed-loop control of power and temperature in multi-core processors.

The tutorial will assume the audience has no background in classical or modern control theory or techniques. It will use the power capping problem and the temperature emergency problem as vehicles for presenting the evolution of closed-loop power and thermal management techniques since the early 2000 until the present.

The tutorial will bring up issues pertinent to closed-loop control systems that are essential for the practical success of control techniques in the context of multi-core power/thermal management. These issues include adaptation to load variations, robustness with respect to power/thermal model uncertainty, response time, constraint satisfaction, and stability.

Although power/thermal management of multi-core chips presents some similarities with that of clusters and data centers, this tutorial will stress some of the major differences and outlines the challenging aspects of the multi-core case, especially in terms of scalability and per-core modeling and control.

Organizer:
Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Tech., IBM Corp., Abu Dhabi, United Arab Emirates*

Speakers:
Charles Lefurgy - *IBM Research - Austin, TX*
Sherief Reda - *Brown Univ., Providence, RI*
Ayse Coskun - *Boston Univ., Boston, MA*

TUT

WEDNESDAY, JUNE 5
6:00 - 7:00pm - Ballroom D

WORK-IN-PROGRESS (WIP)

DAC Work-in-Progress aims to provide authors an opportunity for early feedback on current work and preliminary results.

61.1 Vertical Arbitration-Free 3D NoCs
Ankit More, Siddharth Nilakantan, Mark Hempstead, Baris Taskin - *Drexel Univ., Philadelphia, PA*

61.2 TLM Modelling of 3D Stacked Wide I/O DRAM Subsystems
Matthias Jung - *Univ. of Kaiserslautern, Kaiserslautern, Germany*
Christian Weis, Norbert Wehn - *Technische Univ. Kaiserslautern, Kaiserslautern, Germany*

61.3 Coverage of Compositional Property Sets under Reactive Constraints
Binghao Bao - *Univ. of Kaiserslautern, Kaiserslautern, Germany*
Joerg Bormann - *OneSpin Solutions GmbH, Munich, Germany*
Markus Wedler, Dominik Stoffel, Wolfgang Kunz - *Univ. of Kaiserslautern, Kaiserslautern, Germany*

61.4 Precision Timed Systems Using TickPAD Memory
Matthew Kuo, Partha Roop, **Sidharta Andalam**, Nitish Patel - *Univ. of Auckland, Auckland, New Zealand*

WIP

61.5 Conducting Fast and Accurate MPSoC Virtual Platform Simulation with Parallel Out-of-Order Execution Approach
Yu-Fu Yeh - *Industrial Technology Research Institute, Taipei, Taiwan*
Hsin-Cheng Lin, Chung-Yang (Ric) Huang - *National Taiwan Univ., Taipei, Taiwan*

61.6 Skew-Preserving Discretization Algorithm for Clock Networks with Continuously-Sized Buffers
Amin Farshidi, Logan Rakai, Laleh Behjat, David Westwick - *Univ. of Calgary, Calgary, AB, Canada*

61.7 Dependability Improvement by Partial Reconfiguration in SRAM-Based FPGAs for Critical Applications
Luis Andrés Cardona - *Univ. Autònoma de Barcelona, Bellaterra, Spain*
Yi Guo - *Instituto de Microelectrónica de Barcelona, Spain*
Carles Ferrer - *Univ. Autònoma de Barcelona, Bellaterra, Spain*

61.8 Supporting the Formalization of Requirements Using Techniques from Natural Language Processing
Mathias Soeken, Robert Wille, Eugen Kuksa, Rolf Drechsler - *Univ. of Bremen, Bremen, Germany*

61.9 Troubleshooting Performance Violations at System Level using Data Mining
Lingyi Liu, Xuanyu Zhong - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Xiaotao Chen - *Huawei Technologies Co., Ltd., Bridgewater, NJ*
Shobha Vasudevan - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

61.10 A Design Space Exploration Prototype with Multi-Layer Methodology for Life-Critical Biomedical Engineering Applications
Iyad Al Khatib, Edoardo Paone, Sotirios Xydis, Vittorio Zaccaria, Gianluca Palermo, Cristina Silvano - *Politecnico di Milano, Milano, Italy*

61.11 A General Variable-Latency VLSI Design Methodology Based on Critical Path Identification and Completion Prediction
Kokila Dodda, **Quiyaam Mohammed**, Bao Liu - *Univ. of Texas at San Antonio, TX*

61.12 Work-in-Progress – AgiES: Agile Methods for Embedded System Development
Ville Rantala, Matti Kaisti, Tuomas Mäkilä, Sami Hyrynsalmi, Teijo Lehtonen - *Univ. of Turku, Turun yliopisto, Finland*

61.13 Customized Physical Design for Partitioned On-Chip Memory Module in FPGA
Cong Yan, Peng Li, **Guojie Luo** - *Peking Univ., Beijing, China*

61.14 Queueing Theory Analysis of Memory Architectures
David Dgien, Jiayin Li, Kartik Mohanram - *Univ. of Pittsburgh, Pittsburgh, PA*

61.15 A Multi-Task Scheduling and Allocation Method for Reliable Network-on-Chip
Hiroshi Saito - *Univ. of Aizu, Aizu-Wakamatsu, Japan*
Tomohiro Yoneda - *National Institute of Informatics, Chiyoda-ku, Japan*
Yuichi Nakamura - *NEC Corp., Kawasaki, Japan*

61.16 Extending Run-Time Resource Management to Optimize Heap Memory Utilization of Embedded Applications
Ioannis Koutras, Iraklis Anagnostopoulos - *National Technical Univ. of Athens, Athens, Greece*
Patrick Bellasi - *Politecnico di Milano, Milano, Italy*
Alexandros Bartzas - *National Technical Univ. of Athens, Athens, Greece*
William Fornaciari - *Politecnico di Milano, Milano, Italy*
Dimitrios Soudris - *National Technical Univ. of Athens, Athens, Greece*

61.17 Optimal Dimensioning and Configuration of Electrical Energy Storage Systems for Electric Vehicles
Wanli Chang, **Martin Lukasiewycz**, Sebastian Steinhorst - *TUM CREATE Ltd., Singapore*
Samarjit Chakraborty - *Technical Univ. of Munich, Munich, Germany*

61.18 Understanding the Performance Impacts of Storage Class Memory for I/O-Intensive Workloads
Chia-Lin Yang, Shun-Chih Yu, Yung-En Hsieh, YA-YUNN SU - *National Taiwan Univ., Taipei, Taiwan*
Hsiang-Pang Li - *Macronix International Co., Ltd., Hsinchu, Taiwan*

61.19 FineDedup: A Fine-Grained Deduplication Technique for Flash-Based SSDs
Taejin Kim, Sungjin Lee, Jihong Kim - *Seoul National Univ., Seoul, Republic of Korea*

61.20 Efficient Implementation of Virtual Coarse Grained Reconfigurable Arrays on FPGAs
Karel Heyse, Tom Davidson, Elias Vansteenkiste, Karel Bruneel, **Dirk Stroobandt** - *Ghent Univ., Gent, Belgium*

61.21 A DVFS Framework for Low-Power Embedded GPUs
Daecheol You, Youngho Ahn, Ki-Seok Chung - *Hanyang Univ., Seoul, Republic of Korea*

61.22 BCIBench: A Benchmarking Suite for EEG-Based Brain Computer Interfaces
Ali Ahmadi, Roozbeh Jafari - *Univ. of Texas at Dallas, TX*

61.23 Achieving Timing Closure in Ultra-Low Voltage Designs
Wen-Pin Tu - *Chung Yuan Christian Univ., Chung Li, Taiwan*
Chung-Han Chou - *National Tsing Hua Univ., Hsinchu, Taiwan*
Shih-Hsu Huang - *Chung Yuan Christian Univ., Chung Li, Taiwan*
Shih-Chieh Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yow-Tyng Nieh, Chien-Yung Chou - *Industrial Technology Research Institute, Hsinchu, Taiwan*

61.24 Ant Colony Optimization for Mapping, Scheduling and Placing in Reconfigurable Systems
Antonino Tumeo - *Pacific Northwest National Laboratory, Richland, WA*
Francesco Regazzoni - *Univ. of Lugano, Lugano, Switzerland*

61.25 A Hierarchical Scrubbing Method for Resistance Drift in Multi-Level Cell Phase-Change RAM
Youngsik Kim, **Jina Yoon**, Sungjoo Yoo, Sunggu Lee - *Pohang Univ. of Science and Technology, Pohang, Republic of Korea*

61.26 Simple and Feasible Grid Routing Method for Self-Aligned Quadruple Patterning
Chikaaki Kodama - *Toshiba Corp., Yokohama, Japan*
Hirotaka Ichikawa - *Toshiba Microelectronics Corp., Kawasaki, Japan*
Fumiharu Nakajima, Koichi Nakayama, Shigeki Nojima, Toshiya Kotani - *Toshiba Corp., Yokohama, Japan*

61.27 Power Mananegment Based on Frame Rate for Mobile Virtualization
Youngho Ahn, Daecheol You, Ki-Seok Chung - *Hanyang Univ., Seoul, Republic of Korea*

61.28 Feasibility Analysis for Temperature Constrained Real-Time Scheduling on Multi-Core Platforms
Ming Fan, Vivek Chaturvedi, Shi Sha, Gang Quan - *Florida International Univ., Miami, FL*
Meikang Qiu - *Univ. of Kentucky, Lexington, KY*

61.29 Dynamic Tone Mapping on OLED Display Based on Video Classification
Xiang Chen - *Univ. of Pittsburgh, Pittsburgh, PA*
Zhan Ma, Felix Fernandes - *Samsung, Richardson, TX*
Chun Jason Xue - *City Univ. of Hong Kong, , Hong Kong*
Yiran Chen - *Univ. of Pittsburgh, Pittsburgh, PA*

61.30 Formal Representation of the Design Feature Variety in Analog Circuits
Cristian Ferent, **Alex Doboli** - *State Univ. of New York, Stony Brook, NY*

61.31 Configurable Timing Margin Monitor for Reliability, Test, and Debug
Puneet Sharma, Magdy Abadir - *Freescale Semiconductor, Inc., Austin, TX*

61.32 High Speed Cycle Accurate Simulation for Cache-Incoherent MPSoCs
Christopher Thompson, Miles Gould, Oscar Almer, Nigel Topham - *Univ. of Edinburgh, Edinburgh, United Kingdom*

61.33 A Force-Directed 3D IC Partitioning Algorithm
Aysa Fakheri Tabrizi, Laleh Behjat - *Univ. of Calgary, Calgary, AB, Canada*
William Swartz - *Timberwolf Systems, Inc., Dallas, TX*

61.34 Associative Processing Using Coupled Oscillators
Yan Fang, Donald Chiarulli, Steven Levitan - *Univ. of Pittsburgh, Pittsburgh, PA*

61.35 Extracting Temporal Assertions from Timing Specification Diagrams
Varun Jain, Tim Sherwood - *Univ. of California, Santa Barbara, CA*

61.36 A Novel Time Division Multiplexing Control Mechanism for Bidirectional On-Chip Networks
Chun-jen Wei, Yi-yao Weng - *National Taiwan Univ., Taipei, Taiwan, Taiwan*
Wen-Chung Tsai - *Industrial Technology Research Institute, Hsinchu, Taiwan*
Yuhen Hu - *Univ. of Wisconsin, Madison, WI*
Sao-Jie Chen - *National Taiwan Univ., Taipei, Taiwan*

61.37 Simulation and Analysis of Advanced Network Memory Architectures
Nathan Hunter, Jiayin Li, Kartik Mohanram - *Univ. of Pittsburgh, Pittsburgh, PA*

61.38 Lazy-RTGC: A Real-Time Lazy Garbage Collection Mechanism with Jointly Optimizing Average and Worst Performance for NAND Flash Memory Storage Systems
Qi Zhang, Xuandong Li, Linzhang Wang, Tian Zhang - *Nanjing Univ., Nanjing, China*
Yi Wang, Zili Shao - *Hong Kong Polytechnic Univ., , Hong Kong*

61.39 A Multi-Level Variable Lumping Scheme for Robust Data Modeling in Distributed Sensing Environments
Anurag Umbarkar, **Alex Doboli** - *State Univ. of New York, Stony Brook, NY*

61.40 ILPc: A Novel Approach for Scalable Timing Analysis of Synchronous Programs
JiaJie Wang, Partha Roop - *Univ. of Auckland, Auckland, New Zealand*
Sidharta Andalam - *TUM CREATE Ltd., Singapore*

61.41 Acceleration of SystemC/TLM simulations
Nicolas Ventroux, Julien Peeters, Tanguy Sassolas - *CEA-LIST, Gif-Sur-Yvette, France*
James Hoe - *Carnegie Mellon Univ., Pittsburgh, PA*

61.42 A New SAT-Based Approach for Equivalence Checking of Hardware-Dependent Low-Level Embedded System Software
Carlos Villarraga, Bernard Schmidt - *Technische Univ. Kaiserslautern, Kaiserslautern, Germany*
Joerg Bormann - *OneSpin Solutions GmbH, Munich, Germany*
Dominik Stoffel, Wolfgang Kunz - *Univ. of Kaiserslautern, Kaiserslautern, Germany*

61.43 Design Methodologies for 3D Mixed Signal Integrated Circuits: a Practical 8-bit SAR ADC Design Case
Wulong Liu - *Tsinghua Univ., Beijing, China*
Tao Zhang - *Pennsylvania State Univ., State College, PA*
Xue Han, Yu Wang - *Tsinghua Univ., Beijing, China*
Yuan Xie - *Pennsylvania State Univ., Advanced Micro Devices, Inc., University Park, PA*
Huazhong Yang - *Tsinghua Univ., Beijing, China*

61.44 An Adaptive Instruction Memory for Simultaneous Enhancement of Low Power and High Performance Computing
Yong Kyu Jung - *Adaptmicrosys LLC, Erie, PA*

61.45 Optimization for Static Timing Analysis in Test and Debug
Anatoly Normatov, Pearl Liu, Arie Margulis, Rahul Shukla, **David Akselrod** - *Advanced Micro Devices, Inc., Markham, ON, Canada*

61.46 Dynamic Resolution in Distributed Cyber-Physical System Simulation
Dylan Pfeifer, Jonathan Valvano, Andreas Gerstlauer - *Univ. of Texas at Austin, TX*

61.47 Dynamic Power Reduction with Standard Cells Re-organization During "Logic Synthesis"
Vlinay Adavani - *Infinera Corp., Bangalore, India*

61.48 A Formal Approach to DC Operating Point Analysis for Large Mixed Signal Circuits: Challenges and Opportunities
Parijat Mukherjee - *Texas A&M Univ., College Station, TX*
Chirayu Amin - *Intel Corp., Hillsboro, OR*
Peng Li - *Texas A&M Univ., College Station, TX*

61.49 CyberPhysical System-on-Chip (CPSoC) : A Self-Aware Design Paradigm with Cross-Layer Virtual Sensors and Actuators
Nikil Dutt, Nalini Venkatasubramanian, Alex Nicolau - *Univ. of California, Irvine, CA*
Puneet Gupta - *Univ. of California, Los Angeles, CA*

61.50 Implementing Wireless Communication Links For 3D ICs – The Microbump Way
Julia Lu, Wing-Fai Loke, Dimitrios Peroulis, Byunghoo Jung - *Purdue Univ., West Lafayette, IN*

61.51 High-Level Directives for Efficiently Utilizing Scratchpad Memory
Ayodunni Aribuki - *Univ. of Houston, Houston, TX*
Eric Stotzer - *Texas Instruments, Inc., Stafford, TX*
Ernst Leiss - *Univ. of Houston, Houston, TX*

61.52 Microchips that Repair Themselves
Timothy Turner - *College of Nanoscale Science and Engineering, Albany, NY*

61.53 Bridging EDA and Instrumentation Interfaces and Design Flows
Neal Stollon - *HDL Dynamics, Dallas, TX*

61.54 Non-Deterministic Evaluation of SPICE-like Simulation Algorithms on Distributed Systems
Mansour R. Darabad, Mark Zwolinski - *Univ. of Southampton, Southampton, United Kingdom*

61.55 Pruning in System-Level Design Space Exploration Through MCM Analysis for PPN Networks
Roberta Piscitelli - *Univ. of Amsterdam, Amsterdam, The Netherlands*
Hristo Nikolov - *Leiden Univ., Leiden, The Netherlands*
Andy Pimentel - *Univ. of Amsterdam, Amsterdam, The Netherlands*
Todor Stefanov, Sven van Haastregt - *Leiden Univ., Leiden, The Netherlands*

61.56 The Detection of Malicious Data Attack on NAND Flash Storage System Based on Power Signature
Jie Guo - *Univ. of Pittsburgh, Pittsburgh, PA*
Guangyu Sun - *Peking Univ., Beijing, China*
Chun Jason Xue - *City Univ. of Hong Kong, , Hong Kong*
Hai Li - *Univ. of Pittsburgh, Pittsburgh, PA*

61.57 Distributed Runtime Computation of Constraints for Multiple Inner Loops
Nasim Farahini, Ahmed Hemani - *KTH Royal Institute of Technology, Stockholm, Sweden*
Kolin Paul - *Indian Institute of Technology, New Delhi, India*

61.58 High Density 3D Stacked RRAM Cache Designs
Selvakumaran Vadivelmurugan - *Purdue Univ., West Lafayette, IN*

61.59 Variability Aware Efficient Post-Silicon Validation via Segmentation of Process Variation Envelopes
Prasanjeet Das, Sandeep Gupta - *Univ. of Southern California, Los Angeles, CA*

61.60 Post-Silicon Test Generation with Virtual Prototypes
Kai Cong, Fei Xie, Li Lei - *Portland State Univ., Portland, OR*

61.61 STT-MRAM for Non-Volatile Logic ASIC Applications
Gregory Di Pendina - *Spintec, Grenoble, France*
Guillaume Prenat - *Spintec, CEA-INAC/CNRS/UJF/INPG, Grenoble, France*
Bernard Dieny - *Spintec, Grenoble, France*

61.62 Timing Variation Tolerant Real Time Adaptive Pipelines using Wave Completion Sensing
Jayaram Natarajan, Sahil Kapoor, Varsha Koorapati, Debesh Bhatta - *Georgia Institute of Technology, Atlanta, GA*
Adit Singh - *Auburn Univ., Auburn, AL*
Abhijit Chatterjee - *Georgia Institute of Technology, Atlanta, GA*

61.63 P-Spectrum: A Personalized Smartphone Power Management Technique Based on Real-Time Battery and User Behavior Monitoring
Xiang Chen, Hai Li - *Univ. of Pittsburgh, Pittsburgh, PA*

61.64 iVAMS: Intelligent Metamodel-Integrated Verilog-AMS for Fast Analog Block Optimization
Geng Zheng, Saraju Mohanty, Elias Kougianos - *Univ. of North Texas, Denton, TX*

WIP

61.65 Designing Hardware in the Holodeck
Mathias Soeken, Rolf Drechsler - *Univ. of Bremen, Bremen, Germany*

61.66 Merging Silicon Photonics and Electronics: A Design Challenge
Wim Bogaerts - *Ghent Univ., Ghent, Belgium*
Pieter Dumon - *IMEC, Gent, Belgium*

61.67 Modeling of Retention Time for High Speed Embedded Dynamic Random Access Memories
Swaroop Ghosh - *Univ. of South Florida, Tampa, FL*

61.68 Floorplan Driven Architectures and High-level Synthesis Algorithm for Dynamic Multiple Supply Voltages
Shin-ya Abe, Youhua Shi - *Waseda Univ., Shinjuku-ku, Japan*
Kimiyoshi Usami - *Shibaura Institute of Technology, Koto-ku, Japan*
Masao Yanagisawa, Nozomu Togawa - *Waseda Univ., Tokyo, Japan*

61.69 Design Automation for Large Scale Social Networks
Arun Sathanur, Vikram Jandhyala, Chuanjia Xing - *Univ. of Washington, Seattle, WA*

61.70 Identifying Key Elements of Variability using Heterogeneity Estimation for Fast Redesign
Fahd Shaikh, Wei He, Jonathan Sprinkle, **Janet Roveda** - *Univ. of Arizona, Tucson, AZ*

61.71 Verilog-AMS-POM: Verilog-AMS Integrated POlynomial Metamodelling of a Memristor-Based Oscillator
Geng Zheng, Saraju Mohanty, Elias Kougianos - *Univ. of North Texas, Denton, TX*

61.72 Do We Need Wide Flits in Networks-on-Chip?
Junghee Lee - *Georgia Institute of Technology, Atlanta, GA*
Chrysostomos Nicopoulos - *, Nicosia, Cyprus*
Sung Joo Park, Madhavan Swaminathan, Jongman Kim - *Georgia Institute of Technology, Atlanta, GA*

61.73 An Analog Bus for Low Power On-Chip Digital Communication
Farah Naz Taher, Suraj Sindia, Vishwani Agrawal - *Auburn Univ., Auburn, AL*

61.74 The Invisible Shield: User Classification and Authentication for Mobile Device Based on Gesture Recognition
Kent Nixon, Xiang Chen, Zhi-Hong Mao - *Univ. of Pittsburgh, Pittsburgh, PA*
Kang Li - *Rutgers Univ., Piscataway, NJ*
Yiran Chen - *Univ. of Pittsburgh, Pittsburgh, PA*

61.75 Deadlock Verification in Register Transfer Level Designs of Communication Fabrics
Sebastiaan J.C. Joosten, Julien Schmaltz - *Open Univ. of the Netherlands, Heerlen, The Netherlands*

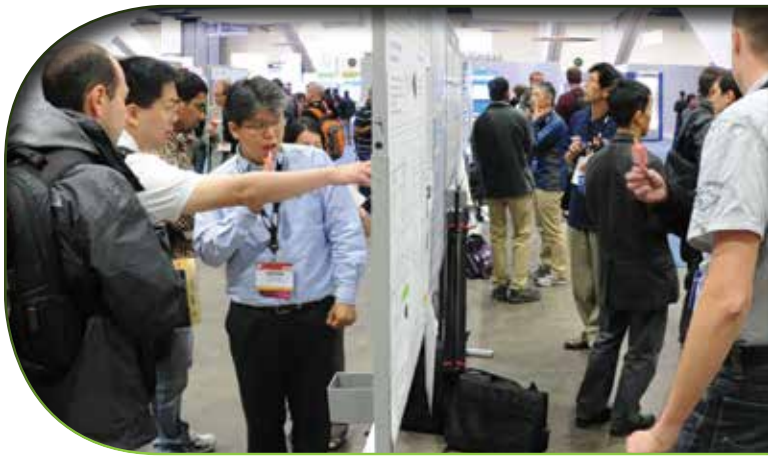
61.76 Yield and Timing Constrained Spare TSV Assignment for Three-Dimensional Integrated Circuits
Yu-Guang Chen - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yiyu Shi - *Missouri Univ. of Science and Technology, Rolla, MO*
Kuan-Yu Lai - *National Tsing Hua Univ., Hsinchu, Taiwan*
Ming-Chao Lee - *Global Unichip Corp., Hsinchu, Taiwan*
Wing-Kai Hon, Shih-Chieh Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*

61.77 Static Low Power Verification in Mixed-Signal SoC Designs
Shubhyant Chaturvedi - *Advanced Micro Devices, Inc., Austin, TX*
Pascal Bolzhauser - *Concept Engineering GmbH, Freiburg, Germany*
Shruti Anand - *Mentor Graphics Corp., Austin, TX*

61.78 Perspective: Practical Application of Thousands of Cores to EDA Problems
Jason Gallia, **Patrick Madden** - *SUNY Binghamton, Binghamton, NY*

61.79 Interchangeable SystemVerilog Random Constraints
Jeremy Ridgeway - *LSI Corp., Milpitas, CA*

61.80 Analytical Task Mapping of Scientific Applications on 3D Network Topologies
Jingjin Wu, Zhiling Lan, **Xuanxing Xiong**, Jia Wang - *Illinois Institute of Technology, Chicago, IL*



A FORMAL APPROACH TO LOW-POWER VERIFICATION

Room: 18D
Verification and Simulation

9:00 - 11:00am

The session addresses how formal methods meet the complex challenges of verifying power-aware SoC designs, which require power optimization throughout the design flow. It demonstrates how formal eases and speeds the analysis, verification and debug at both architecture and RTL levels, ensuring that power management circuitry not only functions correctly, but also does not corrupt the SoC's functionality.

Organizer:
Rob van Blommestein - *Jasper Design Automation, Inc., Mountain View, CA*

Speaker:
Lawrence Loh - *Jasper Design Automation, Inc., Mountain View, CA*

Corporate Supporter: JASPER design automation

WIRELESS ALGORITHM VALIDATION FROM SYSTEM TO RTL TO TEST

Room: 17AB
System Level Design and Communication

IP

2:00 - 4:00pm

Agilent Technologies and Aldec will co-host a session on how to validate a digital signal processing algorithm for both floating and fixed point levels. Attendees will gain insight on cross-domain approach to traditional FPGA design flow and learn how to validate FPGA design for leading edge wireless and radar system with a system-level simulation tool integrated into the traditional hardware design flow.

- Attendees will gain valuable, practical skills with the following tools and equipment:
- Agilent SystemVue as a programming environment to simulate and verify system performance prior to realizing a dedicated hardware implementation.
- Co-simulation interface with Aldec Riviera-PRO for validation of functional blocks described in SystemVue hardware design library.
- HIL (Hardware in the Loop) to accelerate both design validation and test coverage, saving additional development time.

Speakers:
Dmitry Melnik - *Aldec, Inc., Henderson, NV*
Sangkyo Shin - *Agilent Technologies, Inc., Santa Rosa, CA*

Corporate Supporters: ALDEC THE DESIGN VERIFICATION COMPANY

Agilent Technologies

REDUCING DESIGN AND DEBUG TIME WITH SYNTHESIZABLE TLM

Room: 9ABC
High-Level and Logic Synthesis

2:00 - 4:00pm

For teams designing hardware accelerators on an SoC, debugging and integrating the new block is often the most difficult task. For new standards, such as H.265 and Ultra HD TV, companies have moved to synthesizable, transaction-level SystemC to reduce design and debug time.

This session describes an approach to reduce design and debug time of hardware accelerators by 50%. The approach includes:

- Designing synthesizable TLMs in SystemC
- Meeting functional coverage goals in TLMs by using assertions
- What to debug in transactions vs. RTL
- Synthesizing the TLM model into RTL using HLS
- How to use SLEC to formally prove that TLM and RTL match

Speaker:
Bryan Bowyer - *Calypto Design Systems, Wilsonville, OR*

Corporate Supporter: CALYPTO Design · Optimize · Verify

TRACK 1, PART I - SYSTEMVERILOG DESIGN: SYNTHESIS-FRIENDLY SYSTEMVERILOG

Room: 4ABC
Verification and Simulation

Over the past few years SystemVerilog has risen to become the dominant language for constrained random hardware verification, but at the same time SystemVerilog has a lot to offer the hardware designer. SystemVerilog includes a number of significant improvements over Verilog which can be exploited by hardware designers to make their code more concise and readable.

This session will teach you how to use the SystemVerilog language for hardware design by focusing on the parts of the SystemVerilog language that are widely supported by commercial RTL synthesis tools. This session is aimed at engineers who are currently using Verilog or VHDL for RTL design, and who want to start taking advantage of the power of SystemVerilog to better express their hardware design intent.

This track is taught by Doug Smith, Doulos Senior Member, Technical Staff, who has wide experience of teaching SystemVerilog.

Organizer:
Lori Sanine - *Doulos, San Jose, CA*
Speaker:
Doug Smith - *Doulos, Austin, TX*

TRACK 2, PART I - SYSTEMVERILOG VERIFICATION: HARDCORE SYSTEMVERILOG FOR CLASS-BASED VERIFICATION

Room: 8ABC
Verification and Simulation

TS

This session will teach the hardcore object-oriented programming constructs of SystemVerilog as used by methodologies such as UVM. This session is aimed at engineers who have already had some exposure to the SystemVerilog language but are less familiar with object-oriented programming and constrained random verification, and will be a great preparation for the afternoon session on UVM.

Topics to be taught include classes, objects and inheritance, virtual interfaces, functional coverage, randomization and constraints, and more particularly how to use these language features to build a constrained random verification environment that includes a component hierarchy and transaction-level communication.

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

Organizer:
Lori Sanine - *Doulos, San Jose, CA*
Speaker:
John Aynsley - *Doulos, Ringwood, United Kingdom*

TRACK 3, PART I - ARM ACCREDITED ENGINEER PROGRAM: KICK START TO THE ARM CORTEX PROCESSOR FAMILY

Room: 6AB
Embedded Architecture & Platforms

This session will introduce the three CPU architecture variations found in the ARM Cortex Family, highlighting common traits and fundamental differences, and will be of interest to hardware engineers, software engineers and system architects wishing to learn more about ARM processor architecture. This session will discuss the programmers' model, exceptions, memory models and cache architecture and will look at system aspects such as multi-processing with an emphasis on cache coherency issues and interrupt distribution schemes.

The two sessions in this track follow the syllabus of the ARM Accredited Engineer Program, so will be of particular interest to anyone wishing to work toward the AAE exam.

See http://www.arm.com/support/arm-accredited-engineer

This track will be taught by ARM-approved instructors from ARM and from Doulos.

Organizer:
Lori Sanine - *Doulos, San Jose, CA*
Speakers:
David Cabanis - *Doulos, Ringwood, United Kingdom*
Kevin Welton - *ARM Inc., Austin, TX*

ARM ACCREDITATION TRAINING PARTNER

TRACK 4, PART I - ESL AND SYSTEMC - THE DEFINITIVE GUIDE TO SYSTEMC: THE SYSTEMC LANGUAGE

Room: 18D
System Level Design and Communication

SystemC has become well-established as the language of choice for system modelling and virtual platform creation and integration, and is now being applied successfully for high level synthesis. SystemC models also frequently appear as reference models in the hardware verification flow.

This session will provide a solid introduction to the fundamental elements of the SystemC class library, aimed at hands-on hardware or software engineers who might know Verilog or C but have no previous experience of SystemC. This session will also present an overview of how SystemC is being used today in the contexts of system modelling, hardware synthesis, and hardware verification.

This track is taught by David C. Black, Doulos Senior Member, Technical Staff, who is co-author of the book,"SystemC: From the Ground Up."

Organizer:
Lori Sanine - *Doulos, San Jose, CA*
Speaker:
David Black - *Doulos, Austin, TX*

TRACK 1, PART II - SYSTEMVERILOG DESIGN: A HARDWARE DESIGNERS GUIDE TO SYSTEMVERILOG VERIFICATION

Room: 4ABC
Verification and Simulation

Over the past few years SystemVerilog has risen to become the dominant language for constrained random hardware verification, but at the same time SystemVerilog has a lot to offer the hardware designer. SystemVerilog includes a number of significant improvements over Verilog which can be exploited by hardware designers to make their code more concise and readable.

This session will teach you how to use the SystemVerilog language for hardware design by focusing on the parts of the SystemVerilog language that are widely supported by commercial RTL synthesis tools. This session is aimed at engineers who are currently using Verilog or VHDL for RTL design, and who want to start taking advantage of the power of SystemVerilog to better express their hardware design intent.

This track is taught by Doug Smith, Doulos Senior Member, Technical Staff, who has wide experience of teaching SystemVerilog.

Organizer:
Lori Sanine - *Doulos, San Jose, CA*
Speaker:
Doug Smith - *Doulos, Austin, TX*

TRACK 2, PART II - SYSTEMVERILOG VERIFICATION: GETTING STARTED WITH UVM, THE UNIVERSAL VERIFICATION METHODOLOGY

Room: 8ABC
Verification and Simulation

This session will get you started with UVM, the Universal Verification Methodology for SystemVerilog. UVM is an Accellera standard SystemVerilog class library that enables verification code reuse and encourages best practice when building constrained random verification environments.

This session will take a very practical approach to UVM, teaching some of the most common and important features of UVM by presenting a series of fully detailed code examples. This session is aimed at hands-on engineers who want to start writing UVM code themselves and are looking for some specific advice on the best place to start, the right UVM features and coding idiom to use, and the pitfalls to avoid.

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

Organizer:
Lori Sanine - *Doulos, San Jose, CA*
Speaker:
John Aynsley - *Doulos, Ringwood, United Kingdom*

TS

TRACK 3, PART II - ARM ACCREDITED ENGINEER PROGRAM: SOFTWARE DEVELOPMENT FOR THE ARM CORTEX PROCESSOR FAMILY

Room: 6AB
Embedded Software

This session will focus on the software development aspects of the ARM Cortex processor family, and will be of interest to hands-on embedded software engineers targeting ARM Cortex processors, to software engineers transitioning to the ARM Cortex processor from some other processor, and to verification engineers needing to develop test software for ARM-based SoCs.

Topics to be covered include software design tools and methods such as intrinsics, vectorization, and the retargeting of semi-hosted C functions, details of the ARM binary interface and the AAPCS standard, and the synchronisation requirements introduced in the v6/7 architecture. We will discuss software debug aspects and the available hardware infrastructure found in ARM Cortex processors, along with the various Coresight IPs and their relevance to the debug infrastructure. Coding techniques for getting the best results from C code running on an ARM Cortex processor will also be discussed.

This track will be taught by ARM-approved instructors from ARM and from Doulos.

Organizer:
Lori Sanine - *Doulos, San Jose, CA*
Speakers:
David Cabanis - *Doulos, Ringwood, United Kingdom*
Kevin Welton - *ARM Inc., Austin, TX*

ARM ACCREDITED ENGINEER

TRACK 4, PART II - ESL AND SYSTEMC - THE DEFINITIVE GUIDE TO SYSTEMC: TLM-2.0 AND THE IEEE 1666-2011 STANDARD

Room: 18D
System Level Design and Communication

The TLM-2.0 standard has become important in any context that requires communication between transaction-level models, such as within virtual platforms or hardware verification environments. The latest revision of the SystemC standard, IEEE 1666-2011, incorporates the whole of the TLM-2.0 standard as well as adding several significant new features to SystemC.

This session will provide an overview of the TLM-2.0 standard and will explain its significance for anyone interested in transaction-level modelling. This session will also teach some of the new features introduced into SystemC, such as the ability to suspend and resume processes, to create vectors of SystemC objects, and to communicate asynchronously between SystemC and external processes.

This track is taught by David C. Black, Doulos Senior Member, Technical Staff, who is co-author of the book SystemC: From the Ground Up."

Organizer:
Lori Sanine - *Doulos, San Jose, CA*
Speaker:
David Black - *Doulos, Austin, TX*

In addition to DAC's comprehensive technical program, there are other conferences hosting their events at DAC. There is a separate registration fee to attend these meetings. If you are attending one of the conferences below, your registration does not include entrance to the DAC Exhibit Hall Monday-Wednesday. *Please note that a DAC Conference Registration does not include the colocated conferences. Additional registration fees apply.*

ELECTRONIC SYSTEM LEVEL SYNTHESIS CONFERENCE (ESLsyn)

Room: 15
System Level Design and Communication

Friday, May 31 - Saturday, June 1: 9:00am - 5:00pm

The ever-increasing need for enhanced productivity in designing highly complex electronic systems drives the evolution of design methods beyond traditional approaches. Virtual prototyping, design space exploration and system synthesis are needed to design optimized systems, comprising hardware and software implementations. Electronic system-level (ESL) design promises to provide system architects with the right tools to make the right decisions about the system architecture at early stages of the design process. This includes methodologies and synthesis techniques that are supported by appropriate ESL models. Furthermore, a well-connected ESL-to-implementation design flow is needed.

Overall, designing at higher levels of abstraction coupled with the right tool support is a viable way to better cope with the system design complexity, by increasing code reuse and allowing components to be verified earlier in the design process. The Electronic System Level Synthesis Conference - ESLsyn focuses on automated system design methods that enable efficient modeling, synthesis, exploration and verification of systems from high-level specifications down to lower level implementations.

This conference will provide an overview of existing and emerging solutions provided by both industrial partners (EDA companies) and research institutions in the domain of ESL design and synthesis. It will give an outline of synthesis methods and tools currently available in the market and discuss their applicability, performance, strengths and user experiences. Finally, the event will create a platform to foster discussion and exchange between providers of synthesis technology and industry users, as well as serving as a forum to discuss scientific concepts and paradigms for the future evolution of synthesis methods.

Organizers:
Achim Rettberg - *Oldenburg Univ., Oldenburg, Germany*
Andreas Gerstlauer - *Univ. of Texas at Austin, TX*
Marcio Kreutz - *Univ. Federal Rio Grande do Norte, Natal, Brazil*

Sponsored by: ESLsyn

CC

ACM/IEEE INTERNATIONAL WORKSHOP ON SYSTEM LEVEL INTERCONNECT PREDICTION (SLIP)

Room: 18AB
General Interest

Sunday, June 2: 8:00am - 6:00pm

The general technical scope of the workshop is the design, analysis and prediction of interconnect and communication fabrics in electronic systems. The workshop themes include keynote speech, regular paper sessions with paper discussion panels, interactive poster sessions, panels on hot research topics, and embedded tutorials and invited talks.

Representative technical topics include, but are not limited to: interconnect prediction and optimization at various IC design stages, interconnect design challenges and system-level NoC design, design and analysis of power and clock networks, interconnect architecture of structural designs and FPGAs, interconnect fabrics of many-core architectures, design-for-manufacturing (DFM) techniques for interconnects, high speed chip-to-chip interconnect design, design and analysis of chip-package interfaces, interconnect topologies of multiprocessor systems, 3D interconnect design and prediction, emerging interconnect technologies, sensor networks, and synergies between chip communication networks and networks arising in other contexts.

Organizers:
Mustafa Ozdal - *Intel Corp., Hillsboro, OR*
Rasit Topaloglu - *IBM Corp., Fishkill, NY*
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*
Baris Taskin - *Drexel Univ., Philadelphia, PA*
Tsung-Yi Ho - *National Cheng Kung Univ., Tainan City, Taiwan*
Zhuo Li - *IBM Research - Austin, TX*

Sponsored by: www.SLIPonline.org

IEEE INTERNATIONAL SYMPOSIUM ON HARDWARE ORIENTED SECURITY AND TRUST

Room: 17AB
Security

Sunday, June 2 - Monday, June 3: 8:00am - 6:00pm

Pervasive computing is now penetrating a wider range of domains and applications, including many safety-critical cyber-physical systems that we increasingly depend on. Trusted hardware platforms make up the backbone for successful deployment and operation of these systems. However, recent advances in tampering and reverse engineering show that important challenges in guaranteeing the trust of these components await us. For example, malicious alterations inserted into electronic designs can allow for backdoors into the system.

Furthermore, new forms of attacks that exploit side-channel signals are being developed. Third, intellectual-property protection is becoming a major concern in the globalized, horizontal semiconductor business model.

HOST 2013 is a forum for novel solutions to address these challenges. Innovative test mechanisms may reveal Trojans in a design

before they are able to do harm. Implementation attacks may be thwarted using side-channel resistant design or fault-tolerant designs. New security-aware design tools can assist a designer in implementing critical and trusted functionality, quickly and efficiently.

Organizers:
Ramesh Karri - *Polytechnic Institute of New York Univ., Brookyln, NY*
Farinaz Koushanfar - *Rice Univ., Houston, TX*
Michael Hsiao - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

Speaker:
Ramesh Karri - *Polytechnic Institute of New York Univ., Brooklyn, NY*

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NSF/CRA/CCC WORKSHOP ON EXTREME-SCALE DESIGN AUTOMATION AT DAC

Room: 8ABC
Other

Sunday, June 2 - Monday, June 3: 9:00am - 5:00pm

Over a series of three workshops, participants will discuss a broad set of challenges facing the electronic design community, and how these challenges impact the design and fabrication of new electronic systems (both with conventional CMOS and with emerging technologies). The first workshop will focus on emerging technologies and the interplay between graduate education and the design automation workforce. The second workshop will focus on the challenges of system design with many billions of transistors. The final workshop will unify observations made into a series of milestones, benchmarks, and metrics, to help direct research efforts over the next decade.

Organizers:
Alex Jones - *Univ. of Pittsburgh, Pittsburgh, PA*
Patrick Madden - *SUNY Binghamton, Binghamton, NY*

Sponsored by: National Science Foundation WHERE DISCOVERIES BEGIN

CCC

CC

MICROELECTRONIC SYSTEMS EDUCATION (MSE)

Austin Hilton
General Interest

Sunday, June 2 - Monday, June 3: 9:00am - 5:00pm

The International Conference on Microelectronic Systems Education (MSE) is dedicated to furthering undergraduate and graduate education in designing and building innovative microelectronic systems.

Papers are invited (but not limited to) to the following areas:

- Pedagogical innovations using a wide range of technologies, including nanometer-scale integrated circuits, low-power design, nanotechnology, application-specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), multicore/manycore processors, graphics processing units (GPUs), embedded systems, and wireless sensor networks.
- Educational techniques including novel curricula and laboratories, assessment methods, distance learning, textbooks, and design projects.
- Industry and academic collaborative programs and teaching.
- Preparing students for industry, entrepreneurship, academics, and/or research.

The conference is held in the U.S. on odd years, and in Europe on even years, when it is called the European Workshop on Microelectronics Education (EWME). Both conferences provide excellent opportunities for educators and industry to work together to ensure continued excellence in the field of microelectronic systems.

DESIGN AUTOMATION SUMMER SCHOOL

Room: 9ABC
Design for Manufacturability

Sunday, June 2 - Monday, June 3: 8:00am - 6:00pm

The Design Automation Summer School (DASS) will offer graduate students the opportunity to participate in a two-day intensive course on research and development in design automation (DA). Each topic in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments, and indicate remaining challenges. Interactive discussions and follow-up activities among the participants will be used to reinforce and expand upon the lessons.

The goal of DASS is to broaden often highly focused curriculum in DA that is currently offered at universities. The DASS also complements educational and professional development activities in the electronic design automation arena including scholarships, awards, and outreach projects such as the University Booth, the CADathlon, and the Design Automation Conference (DAC) Ph.D. Forum that have met with tremendous success over the past decade. These programs are intended to introduce and outline emerging challenges, and to foster creative thinking in the next generation of DA engineers. Simultaneously, they also help the students hone their problem solving, programming, and teamwork skills, in addition to fostering long-term collegial relationships.

Organizers:
Eli Bozorgzadeh - *Univ. of California, Irvine, CA; Natasa*
Miskov-Zivanov - *Carnegie Mellon Univ., Pittsburgh, PA*

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IEEE INTERNATIONAL WORKSHOP ON DESIGN FOR MANUFACTURING AND YIELD (DFM&Y)

Room: 18AB
Design for Manufacturability

Monday, June 3: 9:00am - 5:00pm

Increased manufacturing susceptibility in today's nanometer technologies requires up to date solutions for yield optimization. In fact, designing an SoC for manufacturability and yield aims at improving the manufacturing process and consequently its yield by enhancing communications across the design – manufacturing interface. A wide range of Design-for- Manufacturability (DFM), Design-for-Yield (DFY) and Design-for-Test (DFT) methodologies and tools are proposed today. Some of these are leveraged during the back-end design stages, and others have post design utilization, from lithography up to 3D integration, wafer sort, packaging, final test and failure analysis.

These solutions can dramatically impact the business performance of chip manufacturers. They can also significantly affect age-old chip design flows. Using a DFM/DFY/DFT solution is an investment and thus choosing the most cost effective one(s) requires trade-off analysis. The workshop will analyze key trends and challenges in DFM, DFY and DFT methodologies, and provide an opportunity to discuss a range of DFM, DFT and DFY solutions for SoC designs now and in the future, including practical case studies that demonstrate the successes and failures of such solutions.

Organizer:
Will Conley - *Cymer, Inc., San Diego, CA*

Speaker:
Will Conley - *Cymer, Inc., San Diego, CA*

CELUG/EDAC ENTERPRISE LICENSING CONFERENCE

Room: 10AB
General Interest

CC

Wednesday, June 5 - Thursday, June 6: 9:00am - 6:00pm

EDA Licensing providers, ISVs, and users will come together at an event co-located with the Design Automation Conference in Austin, June 5 & 6, 2013. CELUG (Centralized Enterprise Licensing Users Group) and EDAC (EDA Consortium) are co-hosting this two-day event at DAC 2013. This interactive event will focus on Enterprise Licensing, with presentations and panels addressing current and future challenges to making high technology tools and users more productive.

This co-located event will bring together Licensing Solution Providers, Independent Software Vendors face to face for interactive sessions with Enterprise Customers from key industries, including:

Academia
Aerospace
Automotive
Oil and Gas
Semiconductor
Life Sciences
Chemical Analysis
Electronic Test
Electronic Measurement

Planned Agenda Overview:

- **Wednesday June 5:** Enterprise Licensing Presentations
- **Thursday June 6:** Enterprise Licensing Presentations (Cont.)

Organizers:
Lee Levenson - *CELUG, San Jose, CA*
Paul Cohen - *EDA Consortium, Boston, MA*
Robert Gardner - *EDA Consortium, San Jose, CA*

Speaker:
Lee Levenson - *CELUG, San Jose, CA*

Sponsored by:

CELUG Centralized Enterprise Licensing User Group

EDA CONSORTIUM

SOUTHWEST DESIGN FOR TEST CONFERENCE

Room: 9ABC
Design for Manufacturability

Thursday, June 6 - Friday, June 7: 9:00am - 5:00pm

The 10th annual SWDFT, SouthWest DFT and Test Conference, consists of two FREE days; this year shifted to the end of the week, to enable co-location with the 50th DAC, Design Automation Conference, and minimize conference overlap. The first day, June 6th, will be a DFT/Test Tutorial (DFT 101), and is colocated with DAC at the Austin Convention Center. The second day, a mix of Keynote and invited speakers who are experts on DFT and Test related technical topics, will be located at the 4-Star Omni SouthPark Hotel in Austin, Texas. We are honored to have Wally Rhines, Mentor Graphics' CEO as this year's Keynote speaker.

As mentioned, SWDFT is a little different than many of the typical industry conferences and symposiums. This conference is completely FREE to register and attend, honest! Late registration will be available onsite; early registration will be available via the link below. SWDFT continues to be focused on practical solutions and knowledge sharing; SWDFT invites industry leaders to present working solutions that can be applied to today's as well as tomorrow's problems.

Organizer:
Jim Johnson - *SWDFT Conference Chair, Buda, TX*

Speakers:
Carl Barnhart - *SiliconAid Solutions, Austin, TX*
Yiorgos Makris - *Univ. of Texas at Dallas, TX*

Sponsored by: Southwest DFT Conference Austin, Texas

SYNOPSYS PARTNER BREAKFAST: OPTIMIZING IMPLEMENTATION OF PERFORMANCE- AND POWER-BALANCED PROCESSOR CORES

Hilton Grand Ballroom H
Low-Power Design and Power Analysis

Monday, June 3: 7:15 - 8:45am

Hear from experts about engineering trade-offs and best practices when using Design Compiler Graphical and IC Compiler to implement an ARM® Cortex®-A15 dual-core processor optimized first for performance, then power, and a Cortex-A7 quad-core processor optimized first for energy efficiency, then maximum speed.

SYNOPSYS LUNCH: ADVANCE YOUR MIXED-SIGNAL VERIFICATION TECHNIQUES TO THE NEXT LEVEL

Hilton Grand Ballroom G
Analog/Mixed-Signal/RF Design

Monday, June 3: 11:30am - 1:30pm

Hear from experts in SoC, memories and IP about the latest techniques to ensure successful AMS design validation for advanced process nodes. From low power and reliability to mixed-signal verification and memory characterization, you will learn how to further advance your current AMS methodologies for performance and accuracy using the latest Synopsys innovations.

SYNOPSYS LUNCH: THE MANY FACES OF ADVANCED TECHNOLOGY

Hilton Grand Ballroom H
Physical Design

Monday, June 3: 11:30am - 1:30pm

Hear from experts at foundry, processor, wireless and consumer electronics companies who have successfully harnessed technology advancements in place-and-route to address their cutting-edge design challenges, whether they be challenges posed by emerging nodes (16-nm/14-nm FinFET) or the productivity challenge of taping out a complex SoC at established nodes, or the challenge of achieving gigahertz clock speeds, or others

AM

SI2 25TH ANNIVERSARY LUNCH

Room: 9ABC
Other

Monday, June 3: 12:00 - 1:30pm

This complimentary lunch will celebrate Si2's 25th Anniversary of establishing design flow standards for the semiconductor industry. It will feature an important keynote speaker as well as awards to those who contributed greatly to Si2's many successes and longevity in the industry.

There is no charge for attending, but please register here so we can plan properly:

Visit here for more information - http://www.si2.org/?page=1544

DESIGN AND IP MANAGEMENT SYMPOSIUM

Ballroom G
Other

Monday, June 3: 1:30 - 2:30pm

Panelists will discuss their Design and IP management methodologies/ technologies, and the results they have achieved. Topics will also include integration of design and verification management for IP-based design. Audience Q&A to follow panel discussion.

Moderator:
Dean Drako - *IC Manage, Inc.,*
Panelists:
Nigel Foley - *CSR,*
Yaron Kretchmer - *Altera Corp.,*
Shiv Sikand - *IC Manage, Inc.,*
Simon Burke - *Xilinx, Inc.,*

SYSTEM-LEVEL POWER MODELING STANDARDIZATION MEETING

Room: 9ABC
Low-Power Design and Power Analysis

Monday, June 3: 2:00 - 4:00pm

At DAC 2012, Si2 sponsored an industry-wide meeting to gather inputs on system level power modeling. Since then, several Si2 working groups have made significant progress in such areas as, power-aware design flows and multi-level power modeling.

This open event will detail those advances for attendees and encourage them to guide planning for further industry-wide standardization efforts.

Discussion will include methods to effectively coordinate across multiple standards organizations with inter-related goals in system-level power modeling requirements for the industry.

There is no charge for attending, but please register here so we can plan properly: http://www.si2.org/?page=1544

COOLEY'S DAC TROUBLEMAKER PANEL

Ballroom G
Other

Monday, June 3: 3:00 - 4:00pm

Come watch the EDA troublemakers answer the edgy, user-submitted questions about this year's most controversial issues! It's an old style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

Moderator:
John Cooley - *Deepchip*

Panelists:
Joe Costello - *Oasys Design Systems, Inc.*
Joe Sawicki - *Mentor Graphics Corp.*
Mike Gianfagna - *Atrenta Inc.*
Dean Drako - *IC Manage, Inc.*
Gary Smith - *Gary Smith EDA*
Jim Hogan - *Vista Ventures*

ANNUAL Si2 OPEN RECEPTION

Room: 9ABC
Other

Monday, June 3: 4:30 - 6:00pm

This complimentary reception will continue Si2's 25th Anniversary celebration. The new Board of Directors will be introduced, and a status report on Si2 activities and plans will be presented. This is an excellent networking opportunity and refreshments will be provided. There is no charge for attending, but please register here so we can plan properly: http://www.si2.org/?page=1544

SYNOPSYS PRIMETIME SIG EVENT: TECHNOLOGY PANEL – ADVANCED ECO METHODOLOGY

Brazos Hall
Emerging Technologies

Monday, June 3: 6:00 - 9:30pm

AM

This PrimeTime Special Interest Group (SIG) event features a technology panel of timing leaders from various fields. Panelists will share their vision and experiences on advanced ECO methodologies that accelerate design closure on the most advanced technology nodes. The Synopsys PrimeTime SIG is an active community for all PrimeTime users and design engineers who want to stay connected with the latest developments in the field of static timing analysis (STA).

CUSTOMER INSIGHTS: SUCCESS WITH SYNOPSYS GALAXY IMPLEMENTATION PLATFORM

Room: 10AB
Other

Monday, June 3 - Tuesday, June 4, 2013

Join us for highly informative sessions covering the latest design trends, challenges and solutions. Listen to leading industry experts present best practices and their success with Synopsys implementation products. Learn how customers have accelerated innovation for their gigascale, gigaHz+, low power and advanced-geometry design challenges. If you are a design engineer or manager, you won't want to miss these special events!

Check in at Synopsys Booth #947 for dates/times

26TH ACM SIGDA UNIVERSITY BOOTH AT THE 50TH DESIGN AUTOMATION CONFERENCE

Room: 4th Floor
General Interest

Monday, June 3 - Wednesday, June 5, 2013: 10:00am - 5:00pm

This year marks the 26th University Booth at the Design Automation Conference. The booth is an opportunity for university researchers to display their results and to interact with participants at DAC. Presenters and attendees at DAC are especially encouraged to participate, but participation is open to all members of the university community. The demonstrations include new EDA tools, EDA tool applications, design projects, and instructional materials.

Booth Coordinators:
Soonhoi Ha
Baris Taskin
Joe Zambreno
Jeonghee Shin

SYNOPSYS PARTNER BREAKFAST: READY FOR DEPLOYING GLOBALFOUNDRIES' 14XM FINFETS IN MOBILE SOC DESIGN

Hilton Grand Ballroom G
Emerging Design Technologies

Tuesday, June 4: 7:15 - 8:45am

Experts from GLOBALFOUNDRIES and Synopsys will describe the key FinFET design advantages and challenges facing designers of mobile products. Through early cycles of collaboration and learning on FinFET transistor design, semiconductor manufacturing through full EDA enablement and optimized FinFET-ready IP, the two companies are enabling a comprehensive design environment and manufacturing-ready solution for optimized implementations of GLOBALFOUNDRIES' 14XM FinFET offering in advanced SoC designs for mobile products.

SYNOPSYS LUNCH: SOC LEADERS VERIFY WITH SYNOPSYS

Hilton Grand Ballroom H
Other

Tuesday, June 4: 11:45am - 1:45pm

Hear industry experts share their viewpoints on what is driving SoC complexity, how their teams have achieved success, how you can apply their insights on your next project, as well as discussions about the latest developments in the verification landscape and advanced technology.

IEEE CEDA PRESENTS: CYBER-PHYSICAL SYSTEMS: A REHASH OR A NEW INTELLECTUAL CHALLENGE?

Room: 18AB
General Interest

Tuesday, June 4: 12:00 - 1:30pm

Speaker:
Edward Lee - *Univ. of California, Berkeley, CA*

The term cyber-physical systems (CPS) refers to the integration of computation and networking with physical processes. CPS is firmly established as a buzzword du jour. Yet many of its elements are familiar and not altogether new. Is CPS just a rehash of old problems designed to attract new funding? In this talk, I will argue that quite to the contrary, CPS is pushing hard at the frontiers of engineering knowledge, putting severe stress on the abstractions and techniques that have proven so effective in the separate spaces of cyber systems (information and computing technology) and physical systems (the rest of engineering). My argument will center on the role of models, and I will show that questions about semantics of models become extremely challenging when the models are required to conjoin the cyber and the physical worlds.

CEDA
IEEE Council on Electronic Design Automation

IPL ALLIANCE DINNER: IPDKS: A THRIVING PDK STANDARD

Hilton Grand Ballroom G
Automation

AM

Tuesday, June 4: 6:00 - 8:00pm

At the 7th Annual IPL Luncheon, IPL Alliance presenters will highlight the benefits of the interoperable PDK (iPDK) standard and their experiences in developing and deploying foundry iPDKs. The IPL Alliance will also present an update on current and future projects as well as collaboration with other industry initiatives.

A. RICHARD NEWTON YOUNG STUDENT FELLOW PROGRAM

Ballroom D
General Interest

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Tuesday morning, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA PhD Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Welcome breakfast and orientation for A. Richard Newton Young Student Fellow Program
Tuesday, June 4 - 7:30 - 8:30am
Room: 18D

Poster Presentation for A. Richard Newton Young Student Fellow Program
(colocated with PhD Forum)
Tuesday, June 4 - 7:00 - 8:30pm
Ballroom D

Closing Session and Award Ceremony for A. Richard Newton Young Student Fellow Program
Thursday, June 6 - 6:00 - 7:00pm
Room: 12AB

ACM/SIGDA MEMBER MEETING WITH PH.D FORUM & A. RICHARD NEWTON YOUNG STUDENT FELLOWSHIP POSTER SESSION

Ballroom D
General Interest

Tuesday, June 4: 7:00 - 8:30pm

The Ph.D Forum, hosted by SIGDA, is a poster session for senior Ph.D. students to disseminate their dissertation research with interested attendees from industry. The session will provide industry to get a chance to meet students and preview student's research work while the students receive feedback on their work from the attendees.

This year's Ph.D forum will be special because it's co-located with A. Richard Newton Young Student Fellow Program. The Newton Young Fellows, who are relatively junior graduate/senior undergraduate students, will have their posters presenting current research or relevant course work/projects.

The attendees will have ample opportunity to interact with immediate and future rising stars in EDA community. There will be an open SIGDA member meeting with a brief presentation on SIGDA's programs. A light dinner will be served. The meeting is open to all members of the EDA and Embedded Systems community.