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- Webinars on Cloud Computing and Security: This year, ACM launched a free learning webinar series. "The Cloud in Your Hands: Marriage of Cloud Computing with Smart Devices" provides an introduction to the exciting new world of cloud-enabled mobile computing. "Security: Computing in an Adversarial Environment" introduces security fundamentals, describes the security mindset, and highlights the difficulties of achieving security. More topics are planned for this popular series!

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IEEE Council on Electronic Design Automation

TUESDAY, June 5, 12:00 pm - 2:00 pm | Room 303

IEEE CEDA Presents: Digital Analog Design Organizer: Joel Phillips, Cadence Design Systems

Speaker: Mark Horowitz, *Stanford University*

The past 30 years have seen enormous growth in the power and sophistication of digital-design tools, whereas progress in analog tools has been far more modest. Digital tools use many abstractions, letting them validate that the implementations match the functional models, and that the composition of cells matches the composition of those models. Although there are many reasons why this is more difficult for analog circuits, it can be done. To prove this point, this talk explains how to leverage the smooth result surface of analog designs to create ways to formally validate analog models to instances, define analog fault models, and even efficiently explore the effect of process variations.

TUESDAY, June 5, 3:00 pm - 3:45 pm | DAC Pavilion, Booth 310

Heritage Series: Interview with Jim Solomon, Phil Kaufman Award Recipient

Moderator: Steve Ohr, Gartner Inc.

Speaker: Jim Solomon, Xulu Entertainment

The analog-design-tool segment has long lived in the shadow of its dazzling digital-tool counterpart. However, without analog, countless consumer electronics devices would not exist. No one has been more closely associated with the advances in analog tool creation than Jim Solomon, former Phil Kaufman Award recipient. Come and hear Jim illuminate the amazing world of analog design.

THURSDAY, June 7, 11:00 am - 12:00 pm | Rooms 102/103

Keynote: My First Design Automation Conference – 1982

Speaker: C.L. (David) Liu, National Tsing Hua University

2011 Phil Kaufman Award winner David Liu reminisces about his first DAC: "It was June 1982 that I had my first technical paper in the EDA area presented at the 19th Design Automation Conference. It was exactly 20 years after I completed my doctoral study and exactly 30 years ago from today. I would like to share with the audience how my prior educational experience prepared me to enter the EDA field and how my EDA experience prepared me for the other aspects of my professional life."

EXHIBITING COMPANIES Orange Denotes First Time Exhibitors

Company Company	Booth	Company	Booth
Agilent Technologies	313	EDA Cafe-IB Systems	707
Aldec, Inc.	2126	EDXACT SA	1002
Altair Engineering, Inc.	2822	EETimes Live Stream sponsored by Cadence	2829
AMIQ EDA	1804	EnSilica Ltd.	2827
Analog Bits Inc.	2830	Entasys Inc.	630
Analog Rails	2815	Esencia Technologies, Inc.	708
Apache Design, an ANSYS subsidiary	1813	EUROPRACTICE	1709
Applied Simulation Technology	1626	EVE-USA, Inc.	1926
ApS Brno Ltd., Codasip Division	1006	Excellicon Inc.	610
Arasan Chip Systems	701	FishTail Design Automation, Inc.	328
ARM Connected Community® (CC) Pavilion	802	Flexras Technologies	2810
ARM CC - Apache Design, an ANSYS subsidary	802	Forte Design Systems	1430
ARM CC - Atrenta Inc.	802 802	GiDEL Clobal UniChin Corp	1802 2007
ARM CC - Cadence Design Systems ARM CC - Carbon Design Systems	802	Global UniChip Corp. GLOBALFOUNDRIES	303
ARM CC - Carbon Design Systems ARM CC - EVE	802	GLOBALFOUNDRIES Partner - AMD	303
ARM CC - Jasper Design Automation	802	GLOBALFOUNDRIES Partner - Apache Design	303
ARM CC - Mentor Embedded, Mentor Graphics Corp.	802	GLOBALFOUNDRIES Partner - Aragio Solutions	303
ARM CC - Space Codesign Systems, Inc.	802	GLOBALFOUNDRIES Partner - ARM	303
ARM CC - Synopsys, Inc.	802	GLOBALFOUNDRIES Partner - Cadence	303
ARM CC - VWorks	802	GLOBALFOUNDRIES Partner - Catena	303
ARM CC - Zocalo Tech, Inc.	802	GLOBALFOUNDRIES Partner - ChipEstimate.com	303
ARM, Inc.	1414	GLOBALFOUNDRIES Partner - CNSE	303
Aspera	307	GLOBALFOUNDRIES Partner - Infinisim	303
Asygn	1506	GLOBALFOUNDRIES Partner - Lorentz Solution	303
ATEEDA	604	GLOBALFOUNDRIES Partner - Mentor Graphics	303
ATopTech	322	GLOBALFOUNDRIES Partner - Socle	303
Atrenta Inc.	2230	GLOBALFOUNDRIES Partner - Synopsys, Inc.	303
Ausdia Inc.	1505	GLOBALFOUNDRIES Partner - Uniquify	303
austriamicrosystems	1725	Gradient Design Automation	914
Avery Design Systems, Inc.	1117	Helic, Inc.	2702
Axiom Design Automation	1625	Huada Empyran Software	1602
BEEcube, Inc.	519	IC Manage, Inc.	1914
Berkeley Design Automation, Inc. Blue Pearl Software	2509, 2515 714	ICScape Inc.	1602 1710
Bluespec, Inc.	1014	Imera Systems, Inc. Infiniscale	2713
Breker Verification Systems	2501	Infotech Enterprises	1101
Cadence Design Systems, Inc.	1930	Integrand Software	2814
Calypto Design Systems	1226	Intel Corp.	814
Cambridge Analog Technologies	2804	Invarian, Inc.	317
Carbon Design Systems	517	IROC Technologies Corp.	2926
Chip Design - Extension Media	1108	Jaryba, Inc.	1007
ChipPath Design Systems	306	Jasper Design Automation, Inc.	830
ChipEstimate.com	1202	Jedat Inc.	2824
ChipStart LLC	1810	Laflin/Instigate	2808
Ciranova, Inc.	1608, 1708	Library Technologies, Inc.	626
CISC Semiconductor GmbH	1102	Lorentz Solution, Inc.	601
ClioSoft, Inc.	2426	Magillem Design Services	514
CLK Design Automation, Inc.	430	Magwel NV	524
CMP	1826	Menta Menta Craphica Corn	1110
Concept Engineering GmbH	1502 304	Mentor Graphics Corp. Methodics, Inc.	1530 2414
Cortus S.A. Coventor, Inc.	1005	Micro Magic, Inc.	1801
CST of America, Inc.	1805	Mirabilis Design Inc.	1906
DAC Pavilion	310	Missing Link Tools LLC	2811
Dassault Systemes Americas Corp.	1026	Mixel, Inc.	2719
DATE 2013	1109	MOSIS	1119
DeFacTo Technologies	1803	MunEDA GmbH	2014
Design and Reuse	1426	National Instruments Corp.	2912
Dini Group	1010	NEC Corp.	614
DOCEA Power	1702, 1806	Netlist	2707
Dolphin Integration	706	NextOp Software, Inc.	900
Dorado Design Automation, Inc.	2717	Nimbic, Inc.	2526
Doulos	1501	Oasys Design Systems, Inc.	530
Duolog Technologies Ltd.	1520	OpenSystems Media	1104
DXCorr Design Inc.	1120	OpenText	2610
56			

Listing as of May 9, 2012

EXHIBITING COMPANIES

Orange Denotes First Time Exhibitors

Company **Booth** OptEM Engineering Inc. 1113 Orora Design Technologies, Inc. 2803 Oski Technology, Inc. 319, 424 Platform Computing, an IBM Company 2708 PLDA 2714 2802 Posedge Inc. PRO DESIGN Electronic GmbH 705 ProPlus Design Solutions, Inc. 2402 ProximusDA 2826 Pulsic Inc. 1908 Real Intent, Inc. 926 Rocketick Technologies LTD. 606 Runtime Design Automation 1508 S2C Inc. 414 1402 Sagantec SAME 1103 Samsung Electronics 2001 Satin Technologies 2210 Seloco, Inc. 2709 Semifore, Inc. 2314 Si2 1214 Sigrity, Inc. 2226 Silicon Creations, LLC 2818 SKILLCAD Inc. 1909 2513 SmartPlay Inc. Soctronics Inc. 1106 Solido Design Automation Inc. 2410 Sonnet Software, Inc. 2213 Space Codesign Systems Inc. 417 Springer Lobby SpringSoft, Inc. 1030 StarNet Communications 1724 702 Synapse Design 726 SYNAPTIC & TRAMS 1905 Synopsys, Inc. - Corporate 1130,1730 SynTest Technologies, Inc. 1408 SypherMedia International 1009 Tanner EDA 1126 Target Compiler Technologies NV 826 Tektronix 302 Tela Innovations 704 1001 Tiempo TOOL Corp. 416.612 TowerJazz 1105 True Circuits, Inc. 2726 **TSMC** 2430 TSSI - Test Systems Strategies, Inc. 703 Tyndall National Institute DTE Group 309 **UMIC Research Centre** 1008 Uniquify, Inc. 1902 Univa 1503 Vayavya Labs Inc. 710 Vennsa Technologies, Inc. 1901 Verific Design Automation 1807 Verification Academy 1514 Veritools, Inc. 1823 WinterLogic Inc. 1114 Xilinx Inc. 730 **XYALIS** 600 Z Circuit Automation 1115

ARM® CONNECTED COMMUNITY® PAVILION BOOTH 802

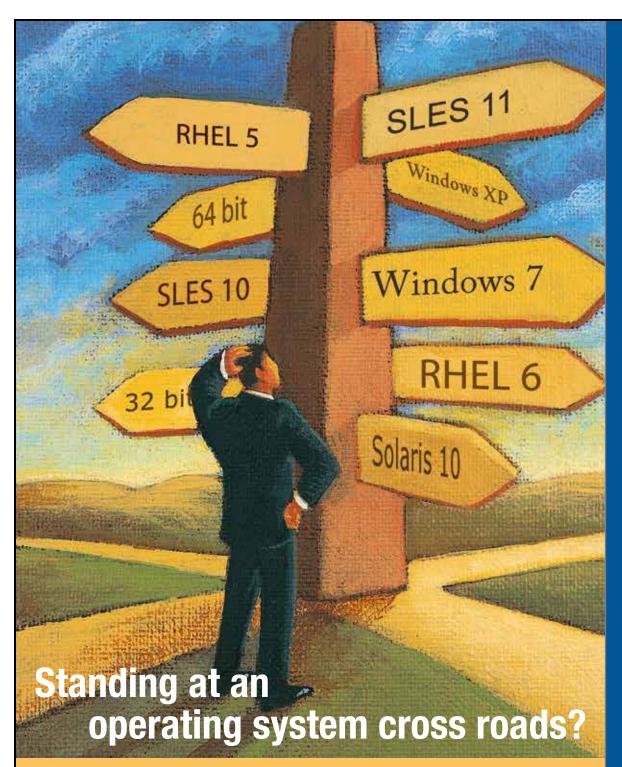


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ARM CC - Apache Design, an ANSYS subsidary	802
ARM CC - Atrenta Inc.	802
ARM CC - Cadence Design Systems	802
ARM CC - Carbon Design Systems	802
ARM CC - EVE	802
ARM CC - Jasper Design Automation	802
ARM CC - Mentor Embedded, Mentor Graphics Corp.	802
ARM CC - Space Codesign Systems, Inc.	802
ARM CC - Synopsys, Inc.	802
ARM CC - VWorks	802
ARM CC - Zocalo Tech, Inc.	802

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Extreme DA	see Synopsys, Inc.
Magma Design Automation, Inc	see Synopsys, Inc.
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? Platinum Exhibitors ?

cadence synopsys 2



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Apache





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ATRENTA



Agilent Technologies

Santa Clara, CA

www.agilent.com

Booth: 313

Agilent EEsof EDA is the leading supplier of Electronic Design Automation (EDA) software for communications product design. Microwave and RF circuit design, high-speed, device modeling, and signal-processing design engineers accelerate the development of better products using design flows built on our system, component, and physics-level design and simulation tools. Visit booth #313 to see the most trusted tools for highly integrated RF circuit simulation and analysis. www.agilent.com/find/eesof.

Aldec, Inc.

Henderson, NV

www.aldec.com **Booth: 2126**

Aldec has been delivering advanced design verification and robust debugging technology to the hardware engineering community for over 25 years. A global EDA company, Aldec offers industry-proven tools to address design verification challenges:

- Active-HDL Simulation/debugging for FPGAs
- Riviera-PRO UVM/OVM based high-end verification methodologies for large ASIC and FPGA designs
- ALINT Design Rule Checking
- HES-Hardware Emulation Solution Simulation/Acceleration
- DO-254 CTS In-hardware Verification
- RTAX/RTSX Rad-tolerant Devices Prototyping

Please visit Aldec at Booth 2126 for a Demo or Technical Session.

Altair Engineering, Inc.

Troy, MI

Booth: 2822

Altair Engineering, Inc., empowers client innovation and decisionmaking through technology that optimizes the analysis, management and visualization of business and engineering information.

Altair's PBS Professional® allows enterprises to easily share distributed computing resources across geographic boundaries. Altair's HyperWorks solution provides best-in-class tools for all facets of the simulation process: modeling, analysis, optimization, visualization, and reporting. With a 26-year-plus track record for high-end software and consulting services, Altair delivers a competitive advantage to customers in a broad range of industries worldwide. To learn more, visit www.altair.com.

AMIQ EDA

Bucharest, Romania

www.dvteclipse.com Booth: 1804

AMIQ EDA focuses on adding value to the design and verification domains through its proprietary code development and analysis tools. The Design and Verification Tools (DVT) platform, the first IDE for e, SystemVerilog, and VHDL, helps engineers increase the speed and quality of code development and simplify legacy code readability and maintenance. Its newer product, Verissimo SystemVerilog Testbench Linter, allows verification groups to improve testbench code reliability and functionality as well as implement best coding practices and their own specific guidelines.

Contact: sales@amiq.com Website: www.dvteclipse.com

Analog Bits Inc.

Mountain View, CA

www.analogbits.com

Booth: 2830 Analog Bits, the integrated clocking and interconnect IP leader, has built an outstanding reputation for "first time working silicon" down to the 28nm node at both merchant foundries and IDMs. Our differentiated products feature the lowest power and smallest footprint in each category. Product lines include precision clocking macros, such as PLLs and DLLs; programmable interconnect solutions, such as multi-protocol SERDES and I/Os; along with specialized high-speed SRAMs and TCAMs and on-die thermometer

Analog Rails

Chandler, AZ

www.analograils.com

Booth: 2815 Analog Rails™ is the key innovator in EDA, accelerating silicon IP delivery by providing designers with an automated, parasitic-aware, Correct By Construction™ approach which revolutionizes analog/ mixed-signal design. Analog Rails™ provides a competitive edge in bringing the best analog/mixed-signal products to market quickly, while drastically reducing cost and schedule creep. Designers efficiently output precision, high-yield analog/mixed-signal IP in hours, rather than days or weeks, enabling first to market delivery for high-end integrated circuits and systems on a chip.

Apache Design, an ANSYS subsidiary

San Jose, CA

www.apache-da.com

Booth: 1813 Apache Design, an ANSYS subsidiary, enables simulation-driven IC and electronic systems design providing chip-level power analysis, optimization, and sign-off solutions. Apache's products advance low-power innovation and address chip-package-system power and noise challenges. Using Apache's simulation software early in the design process enables top semiconductor companies to gain a competitive advantage delivering more power-efficient, highperformance, and noise immune chips. Apache's products lower power consumption, increase performance, mitigate risks, reduce cost, and shorten time-to-market for a broad range of end-markets and applications.

Applied Simulation Technology

San Jose, CA

www.apsimtech.com

Booth: 1626

Applied Simulation Technology offers a comprehensive suite of tools for the modeling and simulation of Electromagnetic effects on PCB, IC package and IC design. This includes Signal Integrity, EMI and Power Integrity for high speed designs. The tool suite includes 2D/3D field solvers, EMI, SI simulators and interfacest to industry standard CAD systems. Model support includes IBIS, SPICE, transmission lines, S parameters in the frequency and time

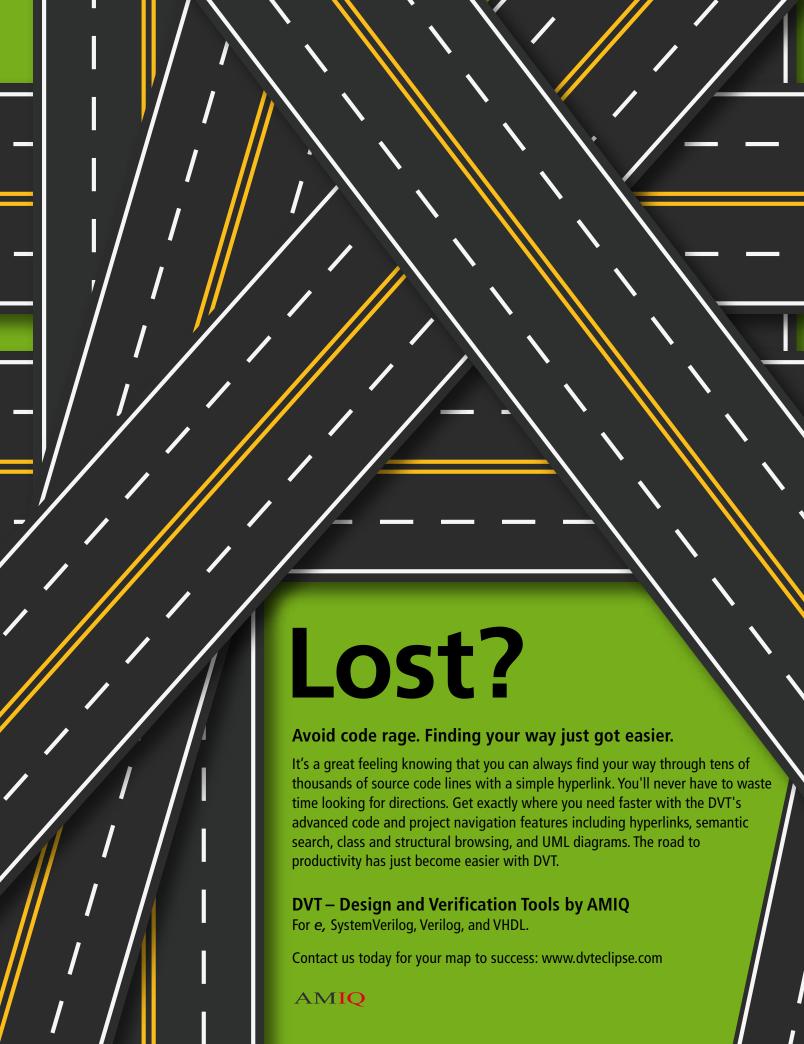
ApS Brno Ltd., Codasip Division

Brno, Czech Republic

www.codasip.com

Booth: 1006

The Codasip® Team is dedicated to assisting the customers with the design and development of application specific instruction-set processors and the corresponding retargetable tools. These tools enable vastly improved efficiency in design space exploration, programming and simulation. By using the Codasip® customizable startup processor platforms and the Codasip® system, one can reduce time-to-market significantly. Codasip® was established in 2006.



Arasan Chip Systems

San Jose, CA

www.arasan.com Booth: 701

Arasan Chip Systems is a leading provider of Total IP solutions for mobile storage and connectivity applications. Arasan's high-quality, silicon-proven, Total IP Solutions include digital IP cores, analog PHY interfaces, verification IP, hardware verification kits, protocol analyzers, software stacks and drivers and optional customization services for MIPI, USB, SD, SDIO, MMC/ eMMC, CF, UFS and many other popular standards.

ARM Connected Community® (CC) Pavilion

San Jose, CA

www.arm.com Booth: 802

The ARM Connected Community is a global network of more than 950 companies aligned to provide a complete solution, from design to manufacture and end use, for products based on the ARM architecture. ARM offers a variety of resources to Community members, including promotional programs and peer-networking opportunities that enable a variety of ARM Partners to come together to provide end-to-end customer solutions. Visit this pavilion to see some of the latest innovations from ARM's EDA and Embedded Partners. www.arm.com/community

ARM CC -Apache Design, an ANSYS subsidary

San Jose, CA

408-457-2000 Booth: 802

Apache Design, an ANSYS subsidiary, enables simulation-driven IC and electronic systems design providing chip-level power analysis, optimization, and sign-off solutions. Apache's products advance low-power innovation and address chip-package-system power and noise challenges. Using Apache's simulation software early in the design process enables top semiconductor companies to gain a competitive advantage delivering more power-efficient, high-performance, and noise immune chips. Apache's products lower power consumption, increase performance, mitigate risks, reduce cost, and shorten time-to-market for a broad range of end-markets and applications.

ARM CC - Atrenta Inc.

San Jose, CA

www.atrenta.com Booth: 802

SpyGlass®, by Atrenta, is the industry-standard platform that makes IP reuse easier, faster and safer. Along with delivering IP health checks and concise DashBoard and DataSheet reports, SpyGlass analyzes and optimizes power, performance, area, testability and overall robustness, ensuring system-on-chip designs are implementation ready. Atrenta's GenSys™ solutions automate platform-based design and chip assembly. Visit us and learn how SpyGlass can help you improve time to market, reduce implementation costs and lower risk.

ARM CC - Cadence Design Systems

San Jose, CA

www.cadence.com Booth: 802

Cadence and ARM have collaborated successfully on the design and verification of high-performance ARM core-based designs across all process nodes. We offer an optimized solution that includes a full set of interoperable technologies with ARM processor and physical IP; services; a system-to-silicon methodology; a mixed-signal solution; and package/board design capabilities. The collaboration enables customers to create innovative electronics faster and with greater confidence that their silicon and systems will get to market on time by providing verified, reusable hardware and software IP blocks.

ARM CC - Carbon Design Systems

Acton, MA

www.carbondesignsystems.com Booth: 802

Carbon Design Systems is a leading provider of virtual prototype and secure virtual model solutions. Carbon's virtual prototype environment enables customers to perform architectural analysis, isolate firmware issues and debug application software problems well in advance of silicon. Carbon is the exclusive provider of implementation accurate virtual models of ARM® IP including the Cortex™-A15, Cortex-A7 and more. System on chip designs validated using technology from Carbon Design Systems are used daily by 100s of millions of people throughout the world.

ARM CC - EVE

San Jose, CA

www.eve-team.com

EVE is the worldwide leader in hardware/software co-verification solutions, offering fast transaction-based co-emulation and in-circuit emulation, with installations at five of the top six semiconductor companies. EVE products shorten the overall verification cycle of complex integrated circuits and electronic systems designs. Its products can be integrated with transaction-level ESL tools and software debuggers, target hardware systems, as well as Verilog, SystemVerilog and VHDL simulators."

Booth: 802

Booth: 802

Booth: 802

ARM CC - Jasper Design Automation

Mountain View, CA

www.jasper-da.com

Jasper delivers industry-leading EDAsoftware solutions for semiconductor design, verification, and reuse, based onstate-of-the-art formal technology. Customers include worldwide leadersin wireless, consumer, computing, and networking electronics. Jasper technologyhas been an integral part of over 150 successful chip deployments. Jasper, headquartered in Mountain View, California, is privately held, withoffices and distributors in North America, South America, Europe, and Asia. Visit www.jasper-da.com to reduce risks, increase design, verification and reuseproductivity; and accelerate time to market.

ARM CC - Mentor Embedded, Mentor Graphics Corp.

Wilsonville, OR

www.mentor.com

Mentor Graphics® is a leader in electronic design automation software. We enable companies to develop better electronic products faster and more cost-effectively. Our innovative products and solutions help engineers conquer design challenges in the increasingly complex worlds of system, board and chip design.





ARM® Connected Community® Pavilion BOOTH #802

A dedicated area on the DAC exhibit floor showcasing ARM's Connected Community (CC) of embedded software and EDA partners.

ARM CC Pavilion Exhibitors as of May 9, 2012



Apache ATRENTA®

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ARM CC - Space Codesign Systems, Inc.

Montreal, QC, Canada

www.spacecodesign.com

oth: 802 ways aspera

Booth: 802

Space Codesign's solution, called SpaceStudio, is advanced software for designing silicon chips that works at a higher level called ESL, or electronic system level. Using SpaceStudio to create their designs, engineers can rapidly evaluate hardware and software options, at the same time, in parallel, and achieve up to 30% reduction in product development time with improved quality.

ARM CC - Synopsys, Inc.

Mountain View, CA

www.synopsys.com

Booth: 802

For 25 years, Synopsys has provided the world's most innovative semiconductor companies with the EDA software, IP and services needed to meet increasingly complex SoC design challenges. Today, the world's leading semiconductor companies rely on Synopsys' comprehensive portfolio of integrated system-level, implementation, verification, IP, manufacturing and FPGA solutions to design their products more quickly and cost effectively with lower risk. Visit Synopsys at DAC or www.synopsys.com to learn about the newest solutions available to help enable the next 25 years of innovation.

ARM CC - VWorks

Adelaide, Australia

www.vworks.com

Booth: 802

VWorks delivers innovative electronic system simulation and virtual prototyping software solutions for embedded software, system and SoC developers. VWorks serves global markets and supply chains for automotive, transportation, mobile, and multimedia electronics and embedded software. ASTC (Australian Semiconductor Technology Company, parent company of VWorks) is a privately-held services company delivering semiconductor design, integration, software development and other services. VWorks and ASTC are headquartered in Adelaide, Australia, with over 100 staff, and offices in Australia, Europe, Japan, and North America. www.vworks.com

ARM CC - Zocalo Tech, Inc.

Austin, TX

www.zocalo-tech.com

Booth: 802

Zocalo Tech offers Zazz for SVA debug and visual creation. With headquarters in Austin, TX and sales offices in the Bay Area, Zazz is being used at major semiconductor and systems houses and IP suppliers to create and debug assertions and ensure actual behavior matches the intended behavior. Zazz automatically creates a constrained-random test bench for assertion debug (independent of design and testbench) to provide immediate feedback on the behavior allowed by assertions and generates a waveform for viewing.

info@zocalo-tech.com

ARM, Inc.

San Jose, CA

www.arm.com Booth: 1414

ARM designs the technology that lies at the heart of advanced digital products, from wireless, networking and consumer entertainment solutions to imaging, automotive, security and storage devices. ARM's comprehensive product offering includes 32-bit RISC CPU and GPU, software, advanced physical IP including memories, std cells and interconnects, POPs, tools and training services, supported by the industry's broadest partner community. http://www.arm.com.

Emeryville, CA

www.asperasoft.com

Aspera is the creator of next-generation transport technologies that move the world's data at maximum speed regardless of file size, transfer distance and network conditions. Based on its patented fasp™ protocol, Aspera software utilizes existing infrastructures to deliver the fastest, most predictable file-transfer experience. Aspera's technology delivers unprecedented control over bandwidth, complete security and uncompromising reliability. More than 1,300 organizations across a variety of industries on six continents rely on Aspera software for the business-critical transport of their digital assets.

Asygn

Montbonnot, France

www.asygn.com

Asygn is a Grenoble-based startup, specializing in the design and verification of analog/mixed-signal and RF systems. The company delivers application-focused solutions in order to deal with tough issues that traditional, generic approaches cannot handle. Asygn's solutions incorporate their own analog system-level simulators, which provide major performance advantages over, for example, systems based on Verilog-AMS. The company has had notable successes in the following applications: imaging arrays; mobile phone radios; MEMs and NEMs sensors; digital and fractional PLLs; high speed IOs.

ATEEDA

Edinburgh, United Kingdom

www.ateeda.com

Booth: 604

Booth: 1506

Booth: 307

ATEEDA lets you solve SoC test cost, time and access problems. Cut your ADC or DAC test costs by 90% using our EDA tools to configure our tiny Built-in Self-Test IP, now proven in silicon and adopted by an industry leader). Fast, accurate on-chip analog testing - in parallel - even when access is restricted. Whether you have SoC, SiP or AMS test issues, we have the solution. ATEEDA - Cutting the cost of analog test.

ATopTech

San Jose, CA

www.atoptech.com

Booth: 322

ATopTech, founded by leading EDA physical design implementation experts to build the next generation of place and route tools focused on advanced technology nodes including 20nm. Our goal is to provide the fastest turn-around time with the best quality of results. ATopTech's products form a complete netlist-to-GDSII physical design solution, from top level design and prototyping to complete block level design while handling all the complexities of variability such as MCMM and AOCV. Excellent correlation with both timing and physical verification sign-off tools is one of our trademark capabilities!

Atrenta Inc.

Silver Exhibitor

San Jose, CA

www.atrenta.com

Booth: 2230

SpyGlass®, by Atrenta, is the industry-standard platform that makes IP reuse easier, faster and safer. Along with delivering IP health checks and concise DashBoard and DataSheet reports, SpyGlass analyzes and optimizes power, performance, area, testability and overall robustness, ensuring system-on-chip designs are implementation ready. Atrenta's GenSys™ solutions automate platform-based design and chip assembly. Visit us and learn how SpyGlass can help you improve time to market, reduce implementation costs and lower risk.



ATRENTA®

Open Innovation Platform®



A Reason to Celebrate!

Let's face it – assembling an SoC today can give anyone a headache.

TSMC and Atrenta have teamed up to ease the pain.

Through the TSMC Soft IP Alliance, we've already certified IP from ten of the top providers as SpyGlass® Clean.

TSMC customers can now design with greater confidence.

No surprises, less headaches.

Now that's a reason to celebrate.

Date: Monday, Jun 4, 2012 Time: 6:00p.m. to 7:00p.m.

Venue: Moscone Center, Room #303 and Outdoor Terrace



Ausdia Inc.

Sunnyvale, CA

Booth: 1505 www.ausdia.com

Ausdia's Timevision is the industry's only fully-integrated timing constraints and CDC solution capable of verifying 100M instance designs with 1000s of clocks. Timevision uses structural and formal techniques to generate and verify constraints, and leverages the SDC environment to verify clock domain crossings without additional setup. Timevision supports RTL or gate-level netlist for both constraints and CDC, and is silicon-proven with multiple tapeouts down to 28nm.

austriamicrosystems

Raleigh, NC

www.austriamicrosystems.com Booth: 1725

austriamicrosystems is a leading designer and manufacturer of high performance analog ICs, combining 30 years of analog design know-how with state-of-the-art manufacturing and test facilities and production partnerships, austriamicrosystems leverages its expertise in low power and high accuracy to provide industry-leading standard and customized analog products. Operating worldwide with more than 1,200 employees, austriamicrosystems focuses on the areas of power management, sensors & sensor interfaces and mobile infotainment in its markets Consumer & Communications, Industry & Medical and Automotive. austriamicrosystems Full Service Foundry is your analog foundry partner focusing on specialty process technologies like RF-CMOS, High-Voltage CMOS, SiGe-BiCMOS and embedded EEPROM processes. With superior support during the design phase, high-end tools and experienced engineers, austriamicrosystems succeeds to be an attractive analog foundry partner especially for fabless design houses.

Avery Design Systems, Inc.

Andover, MA

www.avery-design.com

Booth: 1117 Avery is a leading provider of intelligent functional verification

solutions. Insight PSYN delivers automatic assertion and coverage synthesis. Insight XVER performs X verification at RT and gatelevels including the automatic elimination of X pessimism.

Insight DFT targets RT-level DFT analysis for SDD fault coverage estimation and automatic test point insertion. Avery has a wide range of proven VIP including robust models, protocol checking, and compliance testsuites for PCI Express, USB, xHCI, UAS/BOT, AXI3/AXI4/ACE/AHB, MIPI/M-PHY/UFS, NVMe, SCSI Express, DDR4/LPDDR3, and SATA.

Axiom Design Automation

Milpitas, CA

www.axiom-da.com

Axiom Design Automation, the leader in Multi-Cpu SystemVerilog simulation, will showcase DesignerUVM, its latest ground breaking UVM debug environment. With features like UVM Schematic, automatic port connectivity, tracing port drivers and receivers, virtual interface mapping to the real interface and through to RTL and automatic transaction capture and dumping, DesignerUVM is the next generation verification debug environment. Visit us at Booth 1625 and find out for yourself how Axiom has helped several companies tape out the most complex chips while significantly reducing their verification budget and time.

BEEcube. Inc.

Fremont, CA

www.beecube.com

Booth: 519 BEEcube provides High-Speed multiple FPGA prototyping and development platforms. BEEcube will be showing its latest product miniBEE. BEEcube's technology targets; Computation/ Algorithm prototyping • High Performance Computing • High-end Signal Processing—MIMO, Radar, SDR, and Signal Intelligence. BEE Systems Offer: Direct DAC/ADC interfaces, Symmetrical Honeycomb™ architecture, High-speed Gigabit Sting I/O™, Monitoring/Control with Nectar OS ™, Trace memory-128GB. BPS™ a hardware/software co-development environment on top of MathWorks Simulink™ framework, along with IP-Stitcher™

Berkeley Design Automation, Inc.

Santa Clara, CA

www.berkelev-da.com Booth: 2509, 2515

Berkeley Design Automation, Inc. is the recognized leader in nanometer circuit verification. The company combines the industry's only unified verification platform, Analog FastSPICE, with exceptional application expertise to uniquely address nm circuit design challenges. Over 100 companies, including most of the world's top 20 semiconductor suppliers, rely on Berkeley Design Automation to efficiently verify their nm-scale circuits.

Blue Pearl Software

Santa Clara, CA

www.bluepearlsoftware.com **Booth: 714**

Blue Pearl Software focuses on solving RTL analysis challenges. Blue Pearl Software Suite offers automatically generated Synopsys Design Constraints (SDCs), offers lint and clock domain crossing (CDC) checking and a Visual Verification Environment. These capabilities reduce the number of iterations required to close timing of multi-language (VHDL, SystemVerilog) designs. The software runs natively on Windows and Linux, and is used for FPGA, ASIC and SOC designs, and works with Synopsys' Synplify Pro® FPGA synthesis software flow. http://www.bluepearlsoftware.com.

Bluespec, Inc.

Framingham, MA

www.bluespec.com

Booth: 1014

Bluespec is the Synthesizable Modeling Company(tm). With Bluespec, models and testbenches can be synthesized along with legacy IP to employ emulation much earlier for firmware development, modeling, and verification. When running firmware against design RTL is a must, Bluespec's ARM-based Synthesizable Virtual Platforms are the only solutions delivering high speed, easeof-use, and low cost. Bluespec is powered by the only generalpurpose, high-level synthesis toolset for any use model (models, testbenches, production IP) and design type (datapath, control, interconnect).

Breker Verification Systems

Mountain View, CA

Booth: 1625

www.brekersystems.com Booth: 2501

The stitch-and-ship approach to SoC verification is insufficient for full-SoC designs. Existing block-level testbench-based verification approaches break down for system-on-chip (SoC) designs containing embedded processors. SoC verification requires automated self-verifying C test cases running on the embedded processors to exercise a wide range of functional scenarios. These scenarios ensure that the SoC can support the necessary concurrency, system-level, and software functionality while meeting performance requirements. Breker Verification Systems, The SoC Verification Company, provides this solution with TrekSoC





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Cadence Design Systems, Inc.

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San Jose, CA

www.cadence.com

Cadence is a global leader in software and hardware design tools, silicon intellectual property, and design services that are transforming the electronic design automation (EDA) industry. The Cadence vision for this transformation is called EDA360 because it embraces the entire spectrum of the design process and focuses on end-product profitability. This applications ("app")-driven approach to creating, integrating, and optimizing electronic designs helps our customers realize silicon chips, system-on-chip devices, and complete systems at lower costs and with higher quality. Learn more at www.cadence.com.

Calypto Design Systems

Santa Clara, CA

www.calypto.com

Calypto Design Systems delivers design, optimization and verification software for creating high-quality ASIC and FPGA designs. Calypto is the only company to offer; a patented deep sequential analysis engine for automatic RTL power optimization across the entire SoC design, the industry's #1 high-level synthesis tool for SystemC and C++ synthesis, and an integrated formal equivalence capability that dramatically reduces overall verification effort. See what is new with Calypto's products - PowerPro, Catapult and SLEC - at booth 1226.

Cambridge Analog Technologies

Chelmsford, MA

www.cambridgeanalog.com Booth: 2804

Cambridge Analog Technologies, a subsidiary of Maxim Integrated Products, is a developer of extreme low power high performance analog circuits and IP including analog-to-digital converters, digital-to-analog converters, and phase-lock-loops catering to SoCs built for a wide array of applications including wireless in the cellular, medical and automotive areas, high speed wireline, high end displays, and medical imaging.

Carbon Design Systems

Acton, MA

www.carbondesignsystems.com Booth: 517

Carbon Design Systems is a leading provider of virtual prototype and secure virtual model solutions. Carbon's unified virtual prototype environment enables customers to perform architectural analysis, isolate firmware issues and debug application software problems well in advance of silicon. System on chip designs validated using technology from Carbon Design Systems are used daily by 100s of millions of people throughout the world.

Chip Design - Extension Media

San Francisco, CA

www.chipdesignmag.com Booth: 1108

Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www. chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design, Low Power Engineering, and Semiconductor Design and Manufacturing Portals offer focused editorial content you won't want to miss. And, be sure to visit www.http://eecatalog.com/for valuable information about all of Extension Media's outstanding technology resources.

ChipPath Design Systems

Cupertino, CA

www.chippath.com

ChipPath is the world's largest aggregator of Semiconductor Knowledge focused on design decisions, rapid time to market and economic tradeoff analysis. One SemantIC Architectural specification can be used to select best SoC, FPGA, FPASSP and ASSP fitting project goals. We get you get to market faster, cheaper, and with greater visibility irrespective of final implementation device.

Booth: 306

Booth: 1202

Booth: 1810

Booth: 1102

ChipEstimate.com

San Jose, CA

www.ChipEstimate.com

The ChipEstimate.com chip planning portal is an ecosystem comprised of over 200 of the world's largest IP suppliers and foundries. These companies all share in the common vision of helping the worldwide electronics design community achieve greater profitability and success. To date, a diverse global audience of over 35,000 users have joined the ChipEstimate.com community and has collectively performed over 145,000 chip estimations. Visit the ChipEstimate.com booth where you can learn about the latest in semiconductor design and verification IP.

ChipStart LLC

Palo Alto, CA

www.chip-start.com

ChipStart - A semiconductor IP company providing high quality, preverified subsystem solutions and services for ASIC and Fabless semiconductor companies developing the critical components for communications, consumer and computer-related products. ChipStart's DAC Pavilion will be highlighted by Memoir Systems (Memory), nSilition (Analog IP), Delta (Design Services), SOFICS (ESD), Evatronix (Solution IP), and ChipStart's innovative SoC System Level IP. Schedule an onsite meeting by visiting us at www. chip-start.com.

Ciranova, Inc.

Santa Clara, CA

www.ciranova.com Booth: 1608, 1708

Ciranova Helix is a device-level automated placement solution for RF, analog, and mixed-signal ICs. A designer using Helix can produce high quality, design-rule-correct layout in a small fraction of the time needed using conventional methods, especially at 28nm and below. Ciranova Helix is fully hierarchical and handles designs with tens of thousands of transistors, enabling floorplanning and placement of entire custom IC blocks. Its output is an OpenAccess database that can be edited in any OpenAccess layout editor.

CISC Semiconductor GmbH

Klagenfurt, Austria

www.cisc.at

CISC Semiconductor is a design and consulting company for industries developing embedded microelectronic systems with extremely short Time-To-Market cycles. Our competences include system design, simulation, verification and optimization of heterogeneous embedded microelectronic systems. The 3rd generation of CISC tool "System

Architect Designer" (SyAD®) is a fully featured simulation based verification environment supporting multi-HDL modeling, automatic test bench generation, black and white box verification, IP-Xact library integration, user access management within an easy to use

co-simulation framework for all major simulators.

The Network For Advanced IC Designers



Magazines

In-depth coverage of all the technical challenges and implementation options that engineers face in the development and manufacturing of today's complex integrated circuits (IC)

Engineers' Guides

Locate vendors and products including IP, ASIC's, FPGA's, SoC, EDA tools, design services and more



System-Local Design System-Local Design Figure 1 by System Local Design Figure 2 by System Local Design Figure 3 by System Local Design Figure 3 by System Local Design Figure 3 by System Local Design Figure 4 by System Local Design Figure 4 by System Local Design Figure 5 by System Local

Websites

Online source for the latest tools, technologies and methodologies to better navigate the challenges that face modern IC design environments

Visit *RF and Microwave Systems*Dedicated to covering modeling, design, IP integration and test of RF and microwave functionality into SoCs www.chipdesignmag.com/RFMW

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ASIC/ASSP Verification End User Survey Results

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www.chipdesignmag.com

ClioSoft, Inc.

Fremont, CA

www.cliosoft.com Booth: 2426

ClioSoft is the premier developer of hardware configuration management (HCM) solutions. The company's SOS design data collaboration platform is built from the ground up to handle the requirements of hardware design flows. The SOS platform enables global team collaboration, design & IP reuse, and efficient management of design data from concept through tape-out. SOS is seamlessly integrated with leading IC design flows - Cadence's Virtuoso® AMS and Custom IC Design, Synopsys' Galaxy Custom Designer, SpringSoft's Laker™ Custom Layout Automation System & Mentor's AMS/Custom IC design. The Visual Design Diff (VDD) engine enables easy identification of changes between two versions of a schematic or layout by graphically highlighting the differences directly in the editors.

CLK Design Automation, Inc.

Littleton, MA

www.clkda.com

Booth: 430

CLK Design Automation is the leader in timing margin analysis and variance analysis. AOCV FX™ delivers library, design and path specific derates tables, Path FX™ provides path based variance analysis. The core FX technology is in production at leading foundries for 40nm, 28nm and 20nm and is in use on low power mobile communication and advanced microprocessors and graphic processors designs. A few of CLK's partners and customers include AMD, CSR, and TSMC. More information can be found at www.clkda. com.

CMP

Grenoble Cedex, France

cmp.imag.fr

Booth: 1826

CMP is a manufacturing broker for ICs and MEMS, for prototyping and low volume production.

Since 1981, 1000 Institutions from 70 countries have been served, 6700 projects have been prototyped through 800 manufacturing runs.

Integrated Circuits are available on CMOS, SiGe BiCMOS, HV-CMOS, CMOS-Opto from STMicroelectronics and Austriamicrosystems down to 28nm, 20 nm FDSOI from CEA-LETI, 3D-IC from TEZZARON/GLOBALFOUNDRIES, and 150nm pHEMT GaAs from TRIQUINT.

MEMS are available on various processes: specific MEMS technologies (MUMPS from MEMSCAP) and bulk micromachining.

Concept Engineering GmbH

Freiburg, Germany

www.concept.de

Booth: 1502

Concept Engineering's debugging and visualization software helps electronic design engineers to easily understand, debug, optimize and document electronic designs. StarVision, RTLvision, GateVision, SpiceVision and SGvision are customizable debugging tools for electronic design engineers. Our automatic schematic generation, navigation and viewing technology Nlview/T-engine is available as software component/library for EDA tool developers. Our technology is used in many fields, including: RTL development, IP reuse, ASIC and SoC design, Analog mixed-signal design, synthesis, verification, post-layout analysis, System/RTL/netlist debugging and visualization.

Cortus S.A.

Montpellier, France

www.cortus.com

Cortus is a technology leader in ultra low-power, silicon efficient 32-bit microcontroller IP cores. The product family consists of four 32-bit modern RISC cores ranging from the entry level APS1 to the floating point FPS6. The APS3 is aimed at low energy applications requiring reasonable computational performance. APS3 offers the best DMIPS/mW and DMIPS/mm2 on the market. APS5 and FPS6 are suitable for more complex multi-core systems with caches. A rich ecosystem of peripherals, development tools and RTOS are available.

Booth: 304

Booth: 1005

Booth: 310

Coventor, Inc.

Cary, NC

www.coventor.com

Coventor is the leading provider of MEMS design automation solutions. Its platform of 3D simulation tools and MEMS expertise significantly reduce the time, cost and effort to optimize performance and bring increasingly complex MEMS devices to market. Coventor's tools combine the capacity and accuracy required for high performance MEMS design and offer an integrated approach to enabling MEMS+IC design. Its solutions are embraced by industry experts who agree that "build and test" is no longer an option as a design platform for MEMS.

CST of America, Inc.

Framingham, MA

www.cst.com Booth: 1805

CST of America, Inc. is the leading supplier of 3D full wave simulation tools worldwide. CST STUDIO SUITE™ aids in the pre-layout design and post-layout verification of PCBs, packages, interconnects transitions and complete systems. Results such as near and far-end cross-talk, TDR, eye diagrams, SPICE models, electric and magnetic field and current flow are generated and can be optimized. All types of native layout can be imported. CST is a Cadence technology partner and 3D simulation can be run directly from Cadence tools.

DAC Pavilion

Louisville, CO

www.dac.com

The DAC Pavilion, Sponsored by GLOBALFOUNDRIES, brings the technical conference to the exhibit floor with a wide variety of panels and presentations featuring twenty technical, business and strategy discussions. Panels include discussions on design topics such as multi-core, low-power design, Analog design, IP, Prototyping and Verification. In addition, the Pavilion offers sessions on the Next Killer App, "Teen Talk" on electronics, and the popular Gary Smith on EDA trends and Jim Hogan on the Learning from Apple and More. See pages 51-53, visit DAC.com or stop by the Pavilion booth 310 for a complete schedule. Presentations are free for all attendees.

Dassault Systemes Americas Corp.

Waltham, MA

www.3ds.com Booth: 1026

High Tech and semiconductors companies have to deal with complex product development, manage large amount of information from an expanding value chain, reduce product launch windows and be on top of compliancy.

Dassault SystÄ mes, the 3DExperience company, is working closely with leading electronics companies providing them with a powerful platform, to help accelerate the rate of innovations needed to stay competitive in the marketplace. 3DS provides Business & People with 3D Life-like Universes to imagine sustainable innovations capable of harmonizing Products, Nature and Life. www.3ds.com/hightech



DAC PAVILION



Get the Story on WHAT'S REAL, WHAT'S COMING AND HOW TO BE PREPARED

The DAC Pavilion is the marquee theatre on the exhibit floor with over 15 different presentations that address technology and business issues in a fast-paced shrt presentation format. These 45-60 minute presentations feature the electronic design industries trendsetters and industry insiders. **Booth #310**

DAC Pavilion brings the technical program to the exhibit floor. Sponsored by:



DATE 2013

Edinburgh, United Kingdom

www.date-conference.com **Booth: 1109**

DATE is the complete event for the European electronic system and test community. A world-leading conference and exhibition, DATE unites 2200 professionals with some 60 exhibiting companies, cutting-edge R & D, industrial designers and technical managers from around the world. As per previous editions the DATE 2013 conference will feature two special days. The technical paper submission is 9 September 2012. Please visit our website for further details.

DeFacTo Technologies

Moirans, France

www.defactotech.com **Booth: 1803**

DeFacTo EDA tools help achieving "Design & DFT" closure at RTL. Several needs are covered by the SIGNOFF and the STAR products: IP Integration, Design Verification & DFT Signoff needs. SIGNOFF is a complete solution for RTL testability evaluation, debug & enhancement. It is daily used by DFT engineers and RTL designers. STAR is a fully customizable RTL editing and verification platform.

Design and Reuse

Grenoble, France

www.design-reuse.com

Founded in 1997, D&R became worldwide leader as web portal (www. design-reuse.com) in IP/SoC field & has 70,000 Absolute Unique Visitors/Month. Recently, D&R opened www.dr-embedded.com for Global Solutions for IP based on Platform, Middleware, Design Centers, Fabless vendors etc. Based on 15 years experience, D&R licenses Java/XML multi-application, enterprise platform offering innovation for Web IP cataloging, CRM for IP providers, Design-Reuse Platform and External IP suppliers management.

Dini Group

La Jolla, CA

www.dinigroup.com

Dini Group provides ASIC prototyping systems with the fastest speed, and the biggest FPGAs. Since 1998 they have helped drive the cost of an ASIC gate from more than one dollar, to less than 1/4 cent. Dini boards are used by most major IC developers, and also supplied by leading EDA firms. From offices in La Jolla, California, Dini Group has shipped over ten billion ASIC gates.

DOCEA Power

Moirans, France

www.doceapower.com Booth: 1702, 1806

DOCEA Power provides methodology and tools for enabling architectural (ESL) level power and thermal distribution estimation, allowing up to 70% saving on power consumption. Aceplorer is a dedicated power and thermal modeling and simulation framework for low power strategies exploration, power budget tracking and faster power management software debug. AceThermalModeler is a tool to generate compact and multiple-input RC thermal models of SoCs, 3D IC assemblies and system-in-packages for fast temperature driven architectural decisions. The thermal model can also be used for dynamic coupled power and temperature simulations in Aceplorer for faster and more accurate power and thermal management software development and debug.

Dolphin Integration

Meylan, France

www.dolphin.fr

Dolphin Integration supplies panoplies of CMOS Silicon IP, starring

Booth: 706

Booth: 2717

Booth: 1520

- high-resolution converters for audio and measurement applications,
- libraries of standard cells, register banks and memories,
- networks of power regulators for whole SoCs,
- 80x51 microcontrollers with a Whirl extension for diverse processing.

Its EDA Solutions, and notably the simulator SMASH, serve as the cornerstone ensuring Right-on-first-pass SoC and most competitive Application Schematics for complete subsystems on PCB.

They provide expertise for logic and mixed-signal SoC Integration on all performances up to physical implementation.

Dorado Design Automation, Inc.

Hsin Chu, Taiwan

www.dorado-da.com

ECO(Engineering Change Order) has long been considered as activities related to design change of integrated circuits. Dorado expands the scope of ECO to be "All the incremental jobs in the ECO Phase of design flow", and commits the team to provide solutions for all ECO issues. Dorado's Tweaker product family covers all possible incremental jobs including Functional ECO, Timing ECO, Power ECO, Metal ECO, and Clock ECO. Tweaker family has been developed with ECO specific architecture and algorithm since day one. It supports 40nm, 28nm, and below.

Doulos

Booth: 1426

Booth: 1010

San Jose, CA

www.doulos.com

Booth: 1501 Doulos is the global leader for the development and delivery of world class training solutions in electronics engineering. Fully independent, Doulos sets the industry standard for the highest quality training programs, covering the needs of hardware designers, embedded software developers and system design and verification specialists implementing complex SoC and FPGA designs. The natural partner for leading tool and technology companies, Doulos schedules classes across the U.S. and Europe and delivers in-house training programs world-wide. For more information, visit http://www.doulos.com.

Duolog Technologies Ltd.

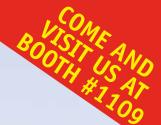
Sandyford - Dublin, Ireland

www.duolog.com

Duolog is a pioneering developer of EDA solutions that enable rapid and error-free SoC integration. Duolog's Socrates integration platform is a correct-by-construction environment for IP, subsystem and system-level integration. Socrates supports current and emerging standards such as IP-XACT and UVM, and auto-generates synchronized views for ESL, hardware, verification and software teams. Socrates delivers major benefits to Duolog's customers eliminating bugs, shrinking design cycles and greatly enhancing inter-team communications.

Founded in 1999, Duolog Technologies has development centers in Ireland and Hungary, with sales and support offices across Europe, the US and Asia.

Conference and exhibition





Alpexpo, Grenoble, France March 18-22, 2013

The 16th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organisation of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results.

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Please visit the DATE website for a list of the topics of interest for DATE 2013.

Submission of Papers

All papers have to be submitted electronically by **Sept 9th, 2012** via: http://www.date-conference.com Papers can be submitted either for standard oral presentation or for interactive presentation.

Chairs

General Chair: Enrico Macii, Politecnico di Torino, Italy, enrico.macii@polito.it

Program Chair: Erik Jan Marinissen, IMEC, Belgium, erik.jan.marinissen@imec.be

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Booth: 707

DXCorr Design Inc.

Sunnyvale, CA

Booth: 1120 www.dxcorr.com

DXCorr is a privately held silicon valley company focused on providing best-in-class embedded solutions- foundation IP- CAMs, memory compilers, standard cells, RTL2GDS2 full-service flow, custom EDA and design automation/ CAD services. DXCorr specializes in power-, performance- and area-optimized IP development, plus high-end chip development services. The company has met the demanding needs of a competitive customer base which includes Tier 1 foundries, IP providers, fabless semiconductor companies and IDMs looking for differentiation.

EDA Cafe-IB Systems

Campbell, CA

www.edacafe.com

Thousands of IC, and system designers visit EDACafé.com to learn about the latest company news and research the latest design tools and services. As the #1 EDA portal it attracts more than 75,000 unique visitors each month and leverages TechJobsCafe.com to bring you targeted job opportunities. EDACafé reaches out to more than 30,000+ EDA professionals with its daily CaféNews. EDACafe will be doing video interviews of industry executives at its DAC booth. Please visit to hear all the conference buzz.

EDXACT SA

Voiron, France

www.edxact.com

Booth: 1002 EDXACT provides high-precision, high-performance technology for backend physical verification. EDXACT is addressing one of the most predominant problems in physical verification: the explosion of data due to an accrued need to cope with parasitic elements. Our task is to bridge the gap between layout extractors, which generate enormous amount of data and simulators, which can no longer cope with that complexity. By ensuring accuracy, together with a substantial decrease in simulation time and memory footprint, circuit designers are now able to gain time and confidence in the results of backend verification.

EnSilica Ltd.

Wokingham, Berkshire, United Kingdom

www.ensilica.com **Booth: 2827**

EnSilica has design centres in Wokingham (UK), Cambridge (UK), and Bangalore (India). EnSilica is focusing on advanced verification of complex semiconductor products and has a portfolio of IP, including a highly configurable 16/32 bit embedded processor called eSi-RISC, the eSi-Comms range of communications IP and eSi-Crypto encryption IP.

The company also provides a full range of IC design services, from System Level Design, RTL coding and verification through to implementation on FPGA devices or ASIC physical design.

Entasys Inc.

Seoul, Republic of Korea

www.entasys.com

Booth: 630 Entasys is an Electronic SystemLevel (ESL) Silicon Virtual Prototyping (SVP) solution provider and its goal isto minimize the painful design iterations from system level chip design to ICimplementations with industry proven breakthrough technologies. This yearEntasys will demonstrate powerful capabilities of pre-RTL SVP and optimal PADconfiguration solution. Pillar-DP-Navis is a pre-RTL SVP solution with lowpower design planning and power/ area/ timing estimation. Optima is aninevitable solution for optimal I/O pad configuration in over 100 million gates SoC designs.

Esencia Technologies, Inc.

San Jose, CA

www.esenciatech.com

The EScala programmable media core is the latest addition to the Esencia Technologies portfolio of specialized IP. The core is fully programmable in C or C++ and the HW can be optimized for particular performance needs. The EScala core technology is designed with full scalability in mind to suit the most demanding embedded applications including video, audio, speech and network

Booth: 708

Booth: 1709

Booth: 1926

Booth: 610

Esencia Technologies also offers full turn-key semi-conductor design services from product specification through GDS2 to production depending on individual client needs. Our team has completed projects for Fortune 500 companies as well as small start-ups in leading semi-conductor process nodes.

EUROPRACTICE

Leuven, Belgium

www.imec.be

The EUROPRACTICE IC Service (IMEC and Fraunhofer) offers low cost ASIC prototyping and small volume fabrication. Low cost prototyping is offered through regularly scheduled Multi Project Wafer runs, whereby several designs are merged onto the same fabrication run,fabricated in CMOS, BiCMOS and SiGe processes from 0.8um to 40nm at ON Semiconductor, austriamicrosystems, IHP, LFoundry, TSMC and UMC. A total design and manufacturing flow is offered including cell library and design kit support, RTL-tolayout, prototyping, volume fabrication, assembly and test.

EVE-USA, Inc.

San Jose, CA

www.eve-team.com

EVE's ZeBu hardware-assisted verification platforms, including its 7th generation ZeBu-Blade2, provide industry leading HW-SW Coverification solutions with the highest performance and the lowest cost-of-ownership in emulation.

Hardware designers and embedded software developers can slash the time and cost of complex SOC development, leveraging ZeBu across the entire design cycle.

ZeBu supports flexible multi-mode emulation, interfacing with Verilog, SystemVerilog and VHDL-based simulators, Electronic-System Level (ESL) tools, and target hardware systems across the range of computer, consumer, networking, communications, and automotive industries.

Excellicon Inc.

Laguna Hills, CA

www.excellicon.com

Done Once! Done Right!

When it comes to Timing Constraints, Excellicon provides the most innovative solution available in the market to date. Correct by Construction approach, along with validate as you design aspect of Excellicon solution eliminates the need for numerous iterations and incomplete verification schemes.

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As the #1 EDA portal, EDACafe.com attracts more than 75,000 unique visitors each month and leverages TechJobsCafe.com to bring you targeted job opportunities. EDACafé reaches out to more than 30,000+ EDA professionals with its daily newsletter. Sign up for our daily newsletter at EDACafe.com.

www.EDACafe.com

FishTail Design Automation, Inc.

Lake Oswego, OR

www.fishtail-da.com

Booth: 328

FishTail Design Automation offers a unique approach to improving chip implementation by automatically generating, merging, promoting and verifying golden timing constraints early in the design cycle. FishTail's products allow designers to drive chip-implementation with complete constraints that are formally proven to be correct and to then manage these constraints as chip-implementation progresses. The result is a shorter chip-implementation schedule with much fewer back-end timing closure iterations. Also, by formally proving the correctness of design constraints you eliminate the risk of silicon failure resulting from incorrect timing exceptions.

Flexras Technologies

Saint-Denis, France

www.flexras.com

Booth: 2810

Wasga Compiler is the implementation and partitioning tool for ASIC/SoC rapid prototyping that provides the highest performances for your multi-FPGA platform within a fast execution time. Wasga Compiler is compatible to any prototyping board with the latest FPGA technologies and it has an unlimited design capacity. Come to see us and attend Wasga demonstrations.

Forte Design Systems

San Jose, CA

www.forteds.com

Booth: 1430

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction and improve design results. Its innovative synthesis technologies and intellectual property offerings allow design teams creating complex electronic chips and systems to reduce their overall design and verification time. More than half of the top 20 worldwide semiconductor companies use Forte's products in production today for ASIC, SoC and FPGA design. Forte is headquartered in San Jose, Calif., with additional offices in England, Japan, Korea and the United States. For more information, visit www.ForteDS.com.

Fractal Technologies LLC

San Mateo, CA

www.fract-tech.com

Booth: 2805

Fractal Technologies is a privately held company with offices in San Carlos, California and Eindhoven, the Netherlands. Fractal Technologies is dedicated to provide high quality solutions and support to enable Customers to validate the quality of internal and external IP's and Libraries. Thanks to our validation solutions, Fractal Technologies maximize value for its Customers either at the Sign Off stage, for incoming inspection or on a daily basis within the Design Flow process.

GIDEL

Santa Clara, CA

www.gidel.com

Booth: 1802 GiDEL provides ASIC/SoC prototyping systems with industry's largest and fastest FPGAs available in the market today. GiDEL's PROCSoC™ is a Modular, Scalable, High Speed Multi-user ASIC prototyping system targeting 6 million to 360 million gates. The system has a distinctive open architecture structure that allows high-volume flexible connectivity to match easily any desired design topology. With enhanced debugging software tool TotalHistory™ effectively a logic analyzer implemented in software, enable designers to debug their FPGA designs in real time. For more information, contact GiDEL in North America at 408-969-0389, or on the web at www.gidel.com

Global UniChip Corp.

Hsinchu City, TW

www.globalunichip.com

GLOBAL UNICHIP CORP. (GUC) is the Flexible ASIC LeaderTM, with 2011 revenue of US\$312 million, who provides an unmatched combination of advanced technology, low power and embedded CPU design capabilities and production knowledge through close partnership with TSMC and major packaging and test companies that are ideal for advanced communications, computing, and consumer electronics applications.

Booth: 2007

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Milpitas, CA

www.globalfoundries.com

GLOBALFOUNDRIES provides advanced semiconductor manufacturing excellence with leading-edge (65nm, 45nm and 28nm) and mature (0.35um to 0.11um) fabrication technologies, on both 200mm and 300mm wafers. GLOBALFOUNDRIES has fabrication facilities in Dresden, New York and Singapore, with a network of design and support centers in Silicon Valley, China, Japan, Germany, Singapore, Taiwan and the U.K. Our support centers include support for design enablement through reference flows and PDKs, as well as silicon proven value added design resources for high voltage and various memory cell types. Visit us at www.globalfoundries.com.

GLOBALFOUNDRIES Partner

- Apache Design

San Jose, CA

www.apache-da.com

Apache Design, an ANSYS subsidiary, enables simulation-driven IC and electronic systems design providing chip-level power analysis, optimization, and sign-off solutions. Apache's products advance low-power innovation and address chip-package-system power and noise challenges. Using Apache's simulation software early in the design process enables top semiconductor companies to gain a competitive advantage delivering more power-efficient, highperformance, and noise immune chips. Apache's products lower power consumption, increase performance, mitigate risks, reduce cost, and shorten time-to-market for a broad range of end-markets and applications.

GLOBALFOUNDRIES Partner -Aragio Solutions

Plano, TX

www.aragio.com

Aragio Solutions is recognized worldwide as a premier provider of innovative I/O Library IP. Aragio's I/O technology, featuring robust ESD protection and high latch-up immunity, enables high performance operation for standard system interfaces (USB 2.0/3.0, DDR2/DDR3, ONFI2/ONFI3, mDDR/LPDDR2, LVDS, SD), and provides ESD protection for RF, Analog, and other high speed interfaces. Partnering with GLOBALFOUNDRIES since 2005, Aragio's delivers silicon-efficient, silicon-verified I/O libraries on 65nm, 55nm, 40nm, and 28nm process nodes. Contact sales@ aragio.com

GLOBALFOUNDRIES Partner - Cadence

San Jose, CA

www.cadence.com

Booth: 303

Cadence is the global leader in software, hardware, IP, and services that is driving the transformation of the EDA industry. With a focus on EDA360, Cadence embraces the entire spectrum of the design process, improving end-product profitability. This application-driven approach for creating, integrating, and optimizing designs helps customers realize silicon chips, system-on-chip devices, and complete systems at lower costs and with higher quality. The EDA360 approach provides a foundation for innovation, creativity and enhanced productivity in the consumer electronics industry and beyond.

GLOBAFOUNDRIES Partner - Catena

Delft, The Netherlands

www.catena.ni

Booth: 303

Catena is a design service and IP provider working with System and IC development for various communication applications; e.g. IEEE802.11abgnp, Bluetooth, GPS, Glonass, FM Broadcast Tuners, TV Tuners and Medical Electronics. Our developments are mainly one chip solutions including RF, Analog, Mixed Signal, DSP and Embedded Software. Catena was founded in the Netherlands in 1986 and is employing 150 skilled engineers. Our customers are both large multinational semiconductor companies and smaller high innovation companies, with whom we have established successful long term cooperation and increased customer revenues. We are working in BiCMOS and CMOS technologies, from 40 nm and up.

GLOBALFOUNDRIES Partner -ChipEstimate.com

San Jose, CA

www.ChipEstimate.com

Booth: 303

The ChipEstimate.com chip planning portal is an ecosystem comprised of over 200 of the world's largest IP suppliers and foundries. These companies all share in the common vision of helping the worldwide electronics design community achieve greater profitability and success. To date, a diverse global audience of over 35,000 users have joined the ChipEstimate.com community and has collectively performed over 145,000 chip estimations. Visit the ChipEstimate.com booth where you can learn about the latest in semiconductor design and verification IP.

GLOBALFOUNDRIES Partner - CNSE

Albany, NY

Booth: 303

The College of Nanoscale Science and Engineering of the University at Albany SUNY is a fully-integrated research, development, prototyping, and educational facility that provides strategic support through outreach, technology acceleration, business incubation, pilot prototyping, and test-based integration support for onsite corporate partners including IBM, Intel, GlobalFoundries, SEMATECH, Samsung, TSMC, Toshiba, Applied Materials, Tokyo Electron, ASML and Novellus Systems, as well as other "next generation" nanotechnology research activities.

GLOBALFOUNDRIES Partner -Infinisim

San Jose, CA

www.infinisim.com

Booth: 303

Are you at 28nm? Is STA is proving to be overly pessimistic? Is On-Chip Variation (OCV) leading to unacceptably large guard banding? Infinisim, through Accurate Dynamic Timing Analysis, overcomes the limitations of STA and provides SPICE accurate timing, power and leakage data, as well as OCV analysis. ClockEdge™, powered by a breakthrough simulation technology (RASER®), guarantees fast, SPICE accurate analysis for the full-clock design. Infinisim suite of products has been successfully deployed at leading semiconductor companies worldwide.

GLOBALFOUNDRIES Partner

-Lorentz Solution

Santa Clara, CA

www.lorentzsolution.com

Lorentz Solution, Inc. develops solutions for high speed analog and RF IC circuit designers. Chances are your smart phone or tablet is built with PeakView designed devices. PeakView is a complete design platform, with an integral full wave electromagnetic field solver, that works to easily create and analyze on-chip passive structures, including caps, inductors, transmission lines and critical interconnect. PeakView is tightly integrated with Virtuoso and Laker on any process or PDK, including advanced processes like 28nm

GLOBALFOUNDRIES Partner

-Mentor Graphics

Wilsonville, OR

www.mentor.com

Mentor EDA solutions provide short design cycle time, improved productivity, and high yield. Products include Vista for virtual prototyping, the Questa verification platform, the Pyxis custom IC design and verification platform, Eldo Premier and ADit for simulation, the Olympus-SoC place and route system, the Calibre PV, Extraction, Advanced Reliability, and DFM platform, and the Tessent suite for comprehensive IC test, failure diagnosis and accelerated yield learning

GLOBALFOUNDRIES Partner -Synopsys, Inc.

Mountain View. CA

www.synopsys.com

Booth: 303 For 25 years, Synopsys has provided the world's most innovative semiconductor companies with the EDA software, IP and services needed to meet increasingly complex SoC design challenges. Today, the world's leading semiconductor companies rely on Synopsys' comprehensive portfolio of integrated system-level, implementation, verification, IP, manufacturing and FPGA solutions to design their products more quickly and cost effectively with lower risk. Visit Synopsys at DAC or www.synopsys.com to learn about the newest solutions available to help enable the next 25 years of innovation.

Gradient Design Automation

Palo Alto, CA

www.gradient-da.com

Booth: 914

Booth: 303

Booth: 303

What if you knew the temperature profile inside your chip-before tapeout? High performance chips have areas with very high power density, causing temperature to rise unevenly within the die. Gradient's HeatWaveT thermal simulator produces a full-chip, threedimensional temperature profile at device- and interconnectlevel resolution. Instance-specific temperatures are annotated into your netlist, giving you thermally-accurate electrical analysis. The designer can pinpoint hotspots and excessive temperature variations-and avoid thermally-induced circuit failures, performance degradations, and reliability issues-before building your chip or 3DIC.

Helic, Inc.

San Francisco, CA

www.helic.com Booth: 2702

Helic, Inc. develops disruptive EDA technologies for RFIC and high-speed SoC design. We provide our customers with a comprehensive offering combining design tools, silicon IP and applications support, greatly reducing the development cycles of chips for wireless communications, broadband networking, PCs, tablets and other segments. We provide technology for rapid electromagnetics modeling, RF component synthesis, and signal integrity of silicon ICs and Systems-in-Package. Our solutions have been adopted by several major semiconductor companies since 2000.

Huada Empyran Software

Beijing, China

www.empyrean.com.cn Booth: 1602

Huada Empyrean Software (HES) is China's largest EDA company. Headquartered in Beijing, with ~300 employees worldwide, HES provides a complete analog/mixed signal design platform and SOC back-end timing closure tools.

IC Manage, Inc.

Las Gatos, CA

www.icmanage.com Booth: 1914

IC Manage provides high performance design and IP management solutions for companies to efficiently collaborate on single and multisite designs. IC Manage lets designers dynamically track, control and distribute library, block-level and SOC design data, including configurations and properties.

Design teams can improve product quality, designer productivity, team collaboration, and bug tracking, plus maximize reuse of existing assets through swift derivations of existing IP. All data authorized for sharing is rapidly accessible worldwide and secured by IC Manage Armor™ protection.

ICScape Inc.

San Clara, CA

www.icscape.com Booth: 1602

ICScape (Santa Clara, CA) develops and markets next generation design closure solutions for SOC designs and an integrated suite of Analog/Mixed Signal design tools for applications including, storage, wireless, data communication, multimedia, image sensor and power management.

ICScape recently became a subsidiary of Huada Empyrean Software (HES - see separate listing), China's largest EDA company. HES is funded by CEC (China Electronic Corporation), the largest electronics company in China.

Visit our booth and talk to our users.

Imera Systems, Inc.

San Jose, CA

www.imera.com

Infiniscale

Montbonnot. France

www.infiniscale.com

InfiniScale comes up with the next-generation solution to variability-aware design challenges for analog, mixed-signal and RF designs. Reputable for its powerful yield optimizer, InfiniScale provides now a comprehensive suite of tools allowing IC designers to efficiently and accurately address statistical verification for advanced technological nodes. An innovative Fast Monte Carlo Analysis with up to 30X, a High-Sigma analysis up to 1000,000X and a unique local variability analysis of devices mismatches or well proximity effects offering designers a real breakthrough technology

Booth: 2713

Booth: 2814

Booth: 814

Booth: 317

Infotech Enterprises

San Jose, CA

www.infotech-enterprises.com Booth: 1101

Infotech Enterprises is a world leader in pure play engineering services with 9,200 employees across 30 locations. Infotech provides concept to silicon and system prototype solutions for ASIC/FPGA Engineering and Embedded Software Development with a 13 year impeccable track record of first pass success on 250+design projects. Infotech's proven and proprietary design flows in silicon engineering enable our customers to shorten their product development cycle which ensures that our customers always stay ahead.

Integrand Software

Berkeley Heights, NJ

www.integrandsoftware.com

Integrand Software's full-wave 3D EM simulation tool EMX®, allows designers to accurately and efficiently simulate large RF circuit blocks, characterize the behavior of passive components and analyze the parasitics due to interconnect. EMX is very fast (seconds for an inductor), very accurate (within a few percent of measurements) and easy to use (seamlessly integrated in Cadence). EMX is widely used for designing inductors, baluns, VCOs, LNAs, packages, bondwires and interconnect and can also generate passive RLCK Spice models from layout.

Intel Corp.

Santa Clara, CA

www.intel.com

Use Intel® CoFluent™ for early system level modeling and simulation of multicore devices. Generate either TLM2 model for SystemC-based virtual platforms or a DML model for WindRiver Simics® for a 5x productivity gain.

Learn about WindRiver Simics®, a full system simulator used by software developers to simulate any target hardware from a single processor to complex electronic systems. Also see a demo of Intel® Platform Profiling Tool where it collects and analyzes Processor/Memory power and temperature.

Invarian, Inc.

Santa Clara, CA

Booth: 1710

www.invarian.com

Invarian's tool suite Pioneer offers industry's most precise signoff analysis solutions for digital and analog designs, its accuracy confirmed by customer's lab measurements.

- Integration of power, thermal, Ir-drop, and EM into a single suite enables unprecedented speed of analysis and ease-of-use.
- Detailed package/environment models used by the tools assure correlation with silicon.
- Flexible input data handling allows tool use from floorplanning to final sign-off.
- Our top-tier users affirm that Pioneer delivers clean tape-out data in a shorter time.

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Booth: 2808

Jaryba, Inc.

Reno, NV

www.jaryba.com

Jaryba is a leading provider of enterprise software for maximizing the utilization of hardware and software assets in clouds, grids and HPC clusters. This enables companies to reduce operation and capital expenses while maintaining the desired application quality of service. Companies around the world rely on Jaryba microScheduler and SmartSuspend to manage the use of server resources and software licenses for interactive and batch workloads, cloud providers, cloudnosted applications and databases. More information about Jaryba is available at www.Jaryba.com.

Jasper Design Automation, Inc.

Mountain View, CA

www.jasper-da.com

Jasper delivers industry-leading EDAsoftware solutions for semiconductor design, verification, and reuse, based onstate-of-the-art formal technology. Customers include worldwide leadersin wireless, consumer, computing, and networking electronics. Jasper technologyhas been an integral part of over 150 successful chip deployments. Jasper, headquartered in Mountain View, California, is privately held, withoffices and distributors in North America, South America, Europe, and Asia. Visit www.jasper-da.com to reduce risks, increase design, verification and reuseproductivity; and accelerate time to market.

Jedat Inc.

Chuo-ku, Tokyo, Japan

www.jedat.co.jp/eng/

Jedat provides the automation of custom layout design with design constraint check and electromigration analysis in the early design stage. With more than 4000 licenses installed worldwide, Jedat's proven technologies have reduced TAT by over 80% compared to conventional design techniques and costly iterations of circuit and layout design.

Some Alpha-SX tools include:

- 1. High performance Analog MOS layout & analyze tools of the Anchor suite
- 2. Ultra high performance Spice waveform viewer
- 3. Hotspot check for terabytes of various layout data formats

Laflin/Instigate

Portland, OR

www.laflinltd.com

Laflin Limited sells/supports EDA tools, IP, and Software Services for leading providers in the electronics industry. Represented at DAC will be Instigate Design, an Armenian software services company, with > 50 successful customer engagements and staff of ~100 engineers. Expertise in virtual prototyping, parallel programming, embedded S/W development, system-level & software design and verification. HOTSCOPE v7.8.0 from JEDAT(/DNP) features its equivalent net trace, schematic viewing of SPICE and EDIF netlists, and LEFDEF net connectivity and element viewing.

Library Technologies, Inc.

Saratoga, CA

www.libtech.com

Exhibiting ChipTimer, design reoptimization for power, timing and power, improving clock speeds by ~30-100%, reducing area by ~10-30% and leakage power by several factors. LibChar for library creation of all flavors, standard cell, IO and memory with integrated job distribution, parallel processing capabilities, CellOpt circuit optimizer for standard cells to reduce power dissipation while meeting timing specs, YieldOpt for variation analysis and cell specific best/worst corner analysis including memories, AgeChar for design specific age dependent library creation and timing analysis.

Booth: 626

Booth: 601

Booth: 514

Booth: 524

Booth: 1110

Lorentz Solution, Inc.

Santa Clara, CA

www.lorentzsolution.com

Lorentz Solution, Inc. develops solutions for high speed analog and RF IC circuit designers. Chances are your smartphone or tablet is built with PeakView designed devices. PeakView is a complete design platform, with an integral full wave electromagnetic field solver, that works to easily create and analyze on-chip passive structures, including caps, inductors, transmission lines and critical interconnect. PeakView is tightly integrated with Virtuoso and Laker on any process or PDK, including advanced processes like 28nm and 20nm.

Magillem Design Services

Paris, France

www.magillem.com

Magillem provides to customers in the electronic industry tools and services that drastically reduce the global cost of complex design. Magillem has developed an easy to use, state of the art platform solution to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SoC. Methodology tools rather than "point" tools: collaborative work, long term Independence, core business oriented platforms.

Magwel NV

Leuven, Belgium

www.magwel.com

Magwel's PTM simulates Rdson, R, current densities, IR drops and dynamic electro-thermal coupling with 3D accuracy in large PMICs and power distribution networks . ESDi extracts and verifies ESD compliance of full-chip ESD networks from layout for all IO pads. SNA models chip-level substrate noise injection (minority and majority carriers), noise coupling and latch-up analysis. DevEM extracts RF parameters for active and passive devices including TSVs and ESD devices.

Menta

Montpellier Cedex 2, France

www.menta.fr

Menta licenses the world's first pure soft embedded-FPGA IP core for SoC. Menta's revolutionary ultra-compact technology increases embedded-FPGA (eFPGA) application range to new levels. This ultra-compact programmable logic architecture provides the post-fabrication flexibility at near ASIC performance. The Menta's FPGA is available in a set of architectures or provided in a highly customizable form. This allows to create domain-specific FPGA giving enormous benefits in terms of Area, Power and Speed.

Booth: 1530

Booth: 1801

Mentor Graphics Corp.

Wilsonville, OR

www.mentor.com

Mentor Graphics is a technology leader in electronic design automation, providing software and hardware design solutions focused on electronic design and physical verification, functional verification, FPGA/PLD, design-for-test, PCB design, embedded software and thermal analysis. Our innovative tools help designers solve current and future design challenges such as scalable solutions for functional verification including emulation; cutting edge technology for design-for-manufacturability and mixed-level IC design verification; award-winning test compression technology; embedded software development systems; and market-leading integrated system design solutions.

Methodics, Inc.

San Francisco, CA

www.methodics-da.com **Booth: 2414**

Methodics, Inc is a leading provider of data management (DM) systems for IC Designers. Methodics solutions include VersIC™ - a revision control solution for Cadence and Synopsys custom design tools; SoC Integrator™ - a generic platform for managing, tracking and assembling SoC content; and IP Developer™ - a unified workspace management and release system for developing digital, analog and software components. Methodics solutions leverage native integrations of the most popular software configuration management systems including Subversion, Perforce, Git, ClearCase and others.

Micro Magic, Inc.

Sunnyvale, CA

www.micromagic.com

Thinking 3D? Micro Magic Inc. is the world's leader in production proven 3D IC tools.

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MAX-3D-FloorPlan automatically optimizes and places TSV's.

MAX-3D-Pathfinder plans 3D designs, then locates and extracts

Micro Magic also provides tools for high-speed datapaths, custom memory design, layout, and analog circuit design.

Mirabilis Design Inc.

Sunnyvale, CA

www.mirabilisdesign.com **Booth: 1906**

Mirabilis Design provides model-based design of SoC and electronics systems for performance optimization, power measurement, and software user-case validation. Using dynamic simulation and graphical model entry, designers can quickly assemble models of their proposed systems using pre-built components, and simulate with workloads and fault injection scenarios. The pre-built reports can be extensively analyzed to make product specification decisions. Demonstrations will cover SoC (Buses, Memories and Processors), Automotive (AUTOSAR and Ethernet), and Aerospace (ARINC 653 and Avionics)

Missing Link Tools LLC

Boulder, CO

www.missinglinktools.com

Missing Link Tools provides software and services to accelerate your time to market and give you confidence in your design. MLT's verification management tool suite, EVOLVE, provides an Agile framework to manage all aspects of your verification & design source control, tests, regressions, releases, coverage and testplans.

Booth: 2811

Booth: 2719

Booth: 2014

With EVOLVE you can identify areas that need more testing, prevent schedule slippage, and tape out sooner. MLT's customers see a 7-15X ROI for their investments with EVOLVE. Contact Missing Link Tools today for a demonstration: info@missinglinktools.com

Mixel, Inc.

San Jose, CA

www.mixel.com

Mixel® is the leader in mixed-signal mobile IPs and offers a wide portfolio of high-performance mixed-signal connectivity IP solutions. Mixel's mixed-signal portfolio employs a LegorithmicTM approach, and includes PHYs and SerDes, such as Mobile PHYs (MIPI® D-PHY, M-PHYSM, and LVDS).

Visit us at the 2012 Design Automation Conference, where Mixel will be showcasing its latest mixed-signal IP such as our D-PHY, and M-PHY products, including the World's First 3D chip integrating five Mixel MIPI IP. Drop your card at Mixel booth #2719 to win an iPod Touch.

MOSIS

Marina del Rey, CA

www.mosis.com

Booth: 1119 From prototype to production, MOSIS is a design engineer's single source for a wide variety of semiconductor processes offered by major foundries (e.g. GF, IBM, TSMC). Costs are kept low by combining designs from many customers into multi-project wafer (MPW) runs. With prototype costs reduced, engineers can submit several variations of the same design to the same run, thus shortening time-to-market. Final designs can then be submitted to MOSIS for low- medium volume production or dedicated Engineering wafer runs (COT). Along with wafers and die, MOSIS provides a full range of packaging and bonding options for designs fabricated through our service.

MunEDA GmbH

Munich, Germany

www.muneda.com

MunEDA develops and licenses EDA tools and solutions that analyze. model, optimize and verify the performance, robustness and yield of analog, mixed-signal and digital circuits. Leading semiconductor companies rely on MunEDA's comprehensive WiCkeD™ tool suite the industry's broadest family of advanced circuit analysis solutions - to reduce circuit design time and achieve maximum yield in their communications, computer, memory, automotive and consumer electronics designs. Founded in 2001, MunEDA is headquartered in Munich, Germany, with offices in Sunnyvale, California, USA (MunEDA Inc.), and leading EDA distributors in the U.S., Japan, Korea, Taiwan, Singapore, Malaysia, Scandinavia, and other countries worldwide. For more information, please visit MunEDA at www.muneda.com.

Booth: 614

National Instruments Corp.

Austin, TX

www.ni.com Booth: 2912

Engineers and scientists use National Instruments graphical system design tools to solve control and automated test challenges. By using NI LabVIEW software to program embedded processors, FPGAs, and reconfigurable I/O within NI hardware devices, design teams can abstract the complexity of their RF designs, embedded prototypes, and measurement systems without sacrificing flexibility and performance. By using off-the-shelf hardware instead of building a custom solution, engineers can prototype and deploy embedded monitoring and control solutions faster. For more information, visit ni.com/labview.

NEC Corp.

Kawasaki, Kanagawa, Japan

www.nec.com

CyberWorkBench, Behavioral C/SystemC synthesis and verification platform, reduces the ASIC/FPGA development time and costs and improves the reliability and quality of the final product. The range of commercial products taped out during the last 20 years goes from network interface circuits, high-speed audio/visual signal processors for high-definition TVs and mobile phones, to cryptographic processors. CyberWorkBench has become an important key to a successful high-tech consumer electronics business that requires a short time-to-market.

Netlist

Irvine, CA

www.netlist.com Booth: 2707

Netlist, Inc. designs and manufactures a suite of high-performance memory subsystems for advanced two processor servers. Significant performance improvements are gained with HyperCloud memory in High Performance Computing applications such as EDA, FEA, CFD, and Data Analytics. HyperCloud memory is qualified on the world's top selling servers.

NextOp Software, Inc.

Santa Clara, CA

www.nextopsoftware.com Booth: 900

NextOp Software is focused on assertion based verification solutions that allow design and verification teams to effectively detect and target RTL bugs. NextOp's assertion synthesis product BugScope automatically generates functional assertions and coverage properties in SVA, PSL and Verilog formats. BugScope fits seamlessly in existing simulation, formal, emulation and acceleration flows.

Nimbic, Inc.

Mountain View, CA

www.nimbic.com Booth: 2526

Nimbic is the leading provider of Maxwell-accurate, 3D Full-Wave Electromagnetic Integrity and SaaS-based Cloud-Computing electronic design automation (EDA) solutions. Nimbic's nWave 3D field solver enables signal integrity (SI), power integrity (PI) and electromagnetic interference (EMI) analysis for chip-package-system co-design as well as 3DIC and Through-Silicon-Via (TSV) design. Nimbic's nCloud scalable cloud compute platform facilitates EM integrity analysis for complex designs cost-effectively and in near real time. Nimbic's global customers include Texas Instruments, Renesas, Toshiba, Qualcomm and Panasonic.

Oasys Design Systems, Inc.

Santa Clara, CA

www.oasys-ds.com

Oasys RealTime Designer brings a new approach to design creation, Chip Synthesis, taking an entire chip design all the way from RTL down to placed gates. The physical RTL synthesis approach is so efficient that designs of hundreds of millions of gates can be processed in a few hours, producing equal or better results than the well-known mainstream synthesis tools take days to achieve. Stop by the Oasys booth and see a demo.

Booth: 530

OpenSystems Media

St. Clair Shores, MI

www.opensystems-publishing.com Booth: 1104

OpenSystems Media has been a leading publisher of electronics magazines, e-mail newsletters, websites, and product resource guides for more than 20 years. OpenSystems Media is also the leader in driving leads and awareness through social media and is the largest producer of lead-generation tools such as webcasts, whitepapers, product directories, Tech E-Briefs, TechChannels, and Techcasts. OpenSystems Media offers E-casts and Techcasts for engineers and provides interactive tools where engineers can communicate directly with presenters and top industry editors. Current publications include: Embedded Computing Design; Military Embedded Systems; CompactPCI, AdvancedTCA, & MicroTCA Systems; DSP-FPGA.com; PC/104 and Small Form Factors; and VITA Technologies. For more information, visit www. opensystemsmedia.com.

OpenText

Richmond Hill, ON, Canada

http://connectivity.opentext.com Booth: 2610

OpenText Connectivity, formerly Hummingbird, offers solutions that allow engineers to maximize the experience of their EDA environment: high-performance remote access to their EDA tools over LAN and WAN, complex 3D application display, team collaboration and productivity features. Find out why 70% of the top semiconductor companies in the world use Exceed onDemand. Come to Booth 2610 to book a customized meeting to discuss your EDA application challenges and enter our daily draws for an XBOX Kinect Bundle!

OptEM Engineering Inc.

Calgary, AB, Canada

www.optem.com Booth: 1113

OptEM Engineering's software and services focus on interconnect design, extraction, modeling and analysis for high-speed analog, digital, and mixed-signal ICs. For deep-submicron ICs, the OptEM Inspector software provides layout-to-circuit device extraction, and 2D/3D substrate and interconnect RC extraction for detailed analysis of crosstalk and delay effects at the cell level. At DAC 2012 we will present our new approach to extracting 3D stack ups, and our highly efficient sensitivity based method for capacitance extraction which models manufacturing variability.

Orora Design Technologies, Inc.

Issaguah, WA

www.orora.com Booth: 2803

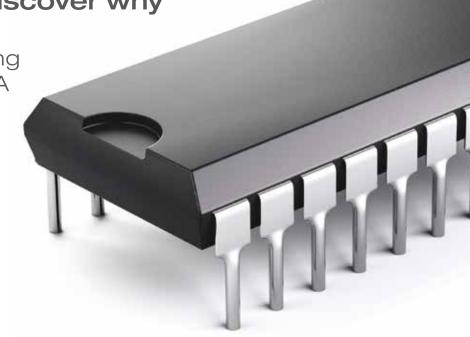
Orora Design Technologies provides an industry-unique platform (Arana) for automatic generation of silicon-faithful Verilog-A/WREAL behavioral models from analog schematics. With the same simulator and the same test benches, Arana speeds up the complex custom-IC simulation and verification by 100x to 1000x, and enables the use of digital simulators to verify mixed-signal designs. Applications include ADCs, DACs, PLLs, High-speed IO, power management circuits, and RFICs. The company also provides a tool (Arsyn) for automated migration and optimization of analog block design.



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Booth: 2802

Oski Technology, Inc.

Mountain View, CA

www.oskitech.com Booth: 319, 424

Oski Technology is the only IC verification services company focused on formal. With 20 years of experience, Oski has pioneered a unique methodology to deliver complete verification solutions that transform the approach to RTL verification, properly integrating formal into traditional simulation-based and coverage-driven flows using simulation-based metrics to define formal coverage, increasing verification coverage and significantly reducing schedule. Oski often finds corner-case bugs almost impossible to detect with simulation. Oski's customers include Cisco, Cypress, NVIDIA, Rambus, Xilinx.

Platform Computing, an IBM Company

Markham, ON, Canada

www.platform.com

Platform Computing, an IBM Company, is a leader in cluster, grid, and cloud management software - serving more than 2,000 of the world's most demanding organizations. For 19 years, its workload and resource management solutions have delivered optimized IT infrastructures, ease of management, and lower costs for enterprise, HPC, and technical computing clients. Visit www.platform.com. Twitter: @Platform_Tweets. For more information about IBM Technical Computing: http://www.ibm.com/deepcomputing.

PLDA

San Jose, CA

www.plda.com

PLDA is a leading provider of semiconductor intellectual property (IP) specializing in high-speed interconnect protocols and technologies. PLDA focuses on high-end IP solutions for the USB and PCI protocol standards and their evolutions (SuperSpeed USB, PCI Express and PCI-X). We offer comprehensive intellectual property (IP) solutions to a global market.

Posedge Inc.

Sunnyvale, CA

www.posedge.com

Posedge is a leading connectivity IP provider of Wireless, Wired Networking, Security and Non-Volatile Memory Interface Solutions. Posedge is truly a Complete Sub-System solution provider offering End to End Hardware, Software drivers, Firmware, and Development boards. Posedge silicon-proven, best in class, high-performance, 802.11n/ac, Application Aware QoS, Wired / Wireless Switching Routing, multi-gigabit protocol level Security, Flash & SD Interconnect Solutions ensure Customer success. Posedge's Semiconductor IP has been licensed by major semiconductor companies.

PRO DESIGN Electronic GmbH

Bruckmuehi, Bavaria, Germany

www.prodesign-europe.com Booth: 705

PRO DESIGN Electronic GmbH is creator of the new proFPGAASIC Prototyping system. The proFPGA system is an modular, highly flexible, scalable and high performance multi FPGA solution. It is scalable in increments of 1 FPGA supporting different FPGA types in one system (Xilinx Virtex7 and Altera Stratix 5). It offers unlimited scalability and max. FPGA IO routing flexibility guaranteeing highest performance. PRO DESIGN has over 80 employees, with various facilities for design, production and sales in Germany.

ProPlus Design Solutions, Inc.

San Jose, CA

www.ProPlusSolution.com

The Silicon Valley-based start-up develops cutting-edge technologies to enhance the linkage between design and manufacturing, and delivers innovative EDA solutions for DFY. It is based on the Device Modeling Platform that has been the choice for leading semiconductor companies since mid-90s, and the Circuit Simulation and DFY Design Platform targeted to meet the challenges of performance and yield trade-offs for advanced circuit designs. ProPlus has R&D centers in both the US and China, branch offices in Tokyo, Hsinchu and Shanghai.

Booth: 2402

Booth: 2826

Booth: 1908

Booth: 926

Booth: 606

ProximusDA

Munich, Germany

www.proximusda.com

Proximusda delivers products for system level architects, verification engineers and embedded software developers facing the heterogeneous distributed computing challenge found in today's SOCs. ProximusDA solutions extend the hardware transaction level methodology to embrace the software side providing a unified transaction level abstraction of the HW/SW system. By leveraging its new fast lightweight parallel task scheduling technology, Proximusda can offer an innovative framework to develop and deploy system level software virtual prototype (SVP) based on multi-cpu/multi-cores distributed execution.

Pulsic Inc.

Santa Clara, CA

www.pulsic.com

Pulsic is the premier provider of physical design tools for custom digital and AMS designs. Pulsic's Unity platform is a fully integrated production-proven solution for floorplanning, placement, and routing of extreme design challenges at advanced nodes. Unity delivers handcrafted quality, faster than manual design. Pulsic has delivered successful tapeouts at 40 nm and below for IDMs and fabless customers in memory, FPGA, custom digital, LCD, imaging, processor and AMS markets worldwide. For more information visit http://www.pulsic.com

Real Intent, Inc.

Sunnyvale, CA

www.realintent.com

Real Intent is the leading provider of software products that accelerate Advanced Sign-off Verification of electronic designs. The company provides comprehensive Clock Domain Crossing solutions for ensuring synchronization between on-chip IP cores, as well as advanced RTL and Constraint Analysis solutions for detecting and eliminating potential complex failure modes of today's highly integrated SoCs. Real Intent's products lead the market in high performance, capacity, report accuracy and comprehensiveness, enabling fast and complete sign-off. For more information, please visit www.realintent.com.

Rocketick Technologies LTD.

Ramat Gan, Israel

www.rocketick.com

Functional verification is a severe bottleneck in chip design projects. Rocketick's flagship product, RocketSim, solves functional verification bottlenecks by complementing simulators with a GPU-based acceleration solution, offering over 10X faster simulations for highly complex designs and 5X server-memory savings. RocketSim offers outstanding coverage and capacity, allowing teams to tape-out more complex products, much earlier, and with much greater confidence.

Runtime Design Automation

Santa Clara, CA

Booth: 1508 www.rtda.com

RTDA helps companies of all sizes meet schedules despite increased design complexities and larger workload. Our family of products enables you to do more with less. LicenseMonitor makes your expensive tool license usage visible. LicenseMonitor also does your next year forecast/budget according to your projects roadmap. NetworkComputer, the fastest job scheduler removes bottlenecks in execution. FlowTracer maximizes design productivity & licenses by deploying fully automated standardized repeatable parallel flows.

S2C Inc.

San Jose, CA

www.s2cinc.com

Booth: 414

S2C will preview its 5th generation products including the new V7 TAI Logic Module family supporting up to 180 million logic gates and the ProtoBridge™ products that facilitate a 500 MB/sec coupling between the verification and prototyping environments.

S2C's products include:

- Rapid Altera and Xilinx-based SoC prototyping hardware
- TAI Player Pro™ prototype design and debug software
- PrototypeReady™ IP and accessories
- ProtoBridge™ expands prototype usage and system verification performance via comodeling through DPI, SCE-MI and C-API

Sagantec

Santa Clara, CA

www.sagantec.com

Booth: 1402 New! 20nm library migration and layout optimization. 100% DRC clean.Sagantec presents a new migration and layout optimization/ correction solution for 20nm. Based on a brand new 2-dimesional

dynamic layout migration engine and designed to work with the challenging new foundry rules of 20nm. Already customer proven with DRC-clean results.

Migrate analog/mixed-signal, memory, library and custom designs to any foundry and process node and cut schedule and effort by an order of magnitude.

SAME

Sophia Antipolis, France

Booth: 1103 www.same-conference.org

SAME: Sophia Antipolis MicroElectronics

SAME: Valorize and promote excellence in the microelectronics sector covering the design technology for advanced electronic circuits in the French Riviera, South of France.

SAME organizes a major European microelectronics event: the SAME Conference, with the support of all major EDA and semiconductor companies.

SAME 2012 Conference: October 2 & 3, 2012 at Sophia Antipolis, France

Main Topic: Innovation in Microelectronics

The SAME 2012 Conference's program is clearly focused on industrial and academic innovation

Information on www.same-conference.org

Samsung Electronics

San Jose, CA

www.samsung.com

Samsung Foundry is dedicated to support fabless and IDM semiconductor companies offering full service solutions encompassing design kits and proven IP to fully turnkey manufacturing to achieve market success with advanced IC designs by Foundry, ASIC and COT engagement. Currently in mass production at 32/28nm, Samsung Foundry is also preparing next generation 20nm and beyond process technologies by leveraging the deep expertise in advanced process technologies, design technologies, as well as a long, proven track record in high-volume manufacturing.

Booth: 2001

Booth: 2210

Booth: 2314

Satin Technologies

Montpellier Cedex 2, France

www.satin-tech.com

Your design monitoring environment deserves more than just scripts and spreadsheets. SatinTech MS™ is a software application that allows you to reinforce your design flow with flexible and automated monitoring capabilities. Whatever your target product (from IP to system) and whatever your design and delivery practices, it is child's play to create checklists and apply them at any design step for automatic validation of key control points. Then results can be shared over the net for more efficient team work.

Seloco, Inc.

Songpa-dong, Songpa-gu, Seoul, Korea

www.seloco.com

Booth: 2709 Since 1990, MyCAD offers a Windows-based EDA toolset which has been installed thousands of copies around the world - USA, Europe, Asia including China and India. Main product for industrial application is MyChip Station, a set of a layout editor and verification tools which have been used for small to medium size design of ICs, LEDs, Opto-devices, MEMs, and LCDs recently. It will also offer a chip-to-layout editing tool. MyCAD's educational set includes VHDL simulator/synthesizer, schematic capture/logic simulator, SPICE simulator and a FPGA experimental kit. Try free at www.mycad.com.

Semifore, Inc.

Mountain View. CA

www.semifore.com

Semifore Inc., "The Addressmap Experts," provides the CSRSpec language and the CSRCompiler, a complete register design solution for hardware, software, verification, and documentation. Collaboratively manage your design from a single source specification. CSRSpec, SystemRDL, IP-XACT, or Spreadsheet inputs generate: Verilog and VHDL RTL; Verilog, or C headers; Perl, IEEE IP-XACT; System Verilog for UVM, VMM and OVM; HTML web pages; and Word or Framemaker documentation. Only Semifore gives your entire team a complete, correct, up-to-date register design ecosystem.

Si₂

Austin, TX

www.si2.org Booth: 1214

Si2 is the largest organization of industry-leading semiconductor, systems, EDA and manufacturing companies focused on the development and adoption of standards to improve the way integrated circuits are designed and manufactured, in order to speed time-to market, reduce costs, and meet the challenges of sub-micron design. Now in its 24th year, Si2 is uniquely positioned to enable timely collaboration through dedicated staff and a strong implementation focus driven by its member companies. Si2 represents over 90 companies throughout the world.

Sigrity, Inc.

Campbell, CA

www.sigrity.com Booth: 2226

Sigrity provides advanced software analysis solutions to ensure power integrity and signal integrity in chips, packages and printed circuit boards; and physical design tools for single die and SiP implementations. Over 250 companies utilize Sigrity products as part of industry standard design flows. Sigrity solutions help companies overcome design challenges and get to market faster while avoiding costly respins and field failures. Sigrity products have won technology innovation awards and the company receives high marks for customer support.

Silicon Creations, LLC

Suwanee, GA

www.siliconcr.com Booth: 2818

Silicon Creations leverages a rich portfolio of PLL and SerDes IP to deliver world class integrated circuit design services and silicon IP. Our Fractional-N PLL with leading jitter performance and wide programmability is silicon proven in over 20 process nodes from 28n to 180n eliminating risk. In full-custom and semi-custom IP or full-chip projects our innovative designs, comprehensive verification flow, rich models and generous support provide our repeat customers with first time right silicon.

SKILLCAD Inc.

San Jose, CA

www.skillcad.com Booth: 1909

SKILLCAD Layout Automation Suite (LAS) provides advanced layout productivity enhancement utilities into Virtuoso. V-Editor/StepRouter minimizes mouse clicks. SKILLCAD Flat Panel Layout Editor (FPLE) offers special utilities for LCD/TFT/Touch screen layout design in Virtuoso. rRouter/rChecker handles hundreds of connections simultaneously with constrains of resistance. SKILLCAD NanoWire Track Editor provides a leading layout solution for routing on track patterns with various via size/orientation configurations in 22nm/20nm technologies.SKILLCAD is seamlessly integrated into Cadence Virtuoso (IC5 & IC6) Platform.

SmartPlay Inc.

San Jose, CA

www.smartplayin.com

SmartPlay Inc. is a leading design services company with expertise in digital, analog, wireless software and system design. With a team of 700+ employees and 6 design centers, SmartPlay is a preferred partner for several semiconductor companies.

Booth: 2513

Booth: 1106

Booth: 2410

SmartPlay has delivered many complex; multimillion gate SoC/ASIC/FPGA's spanning multiple foundries and process nodes including 20/22nm. SmartPlay has successfully engaged and executed projects across the world including U.S., Korea, Malaysia, Japan, China and Taiwan. Second year in a row, SmartPlay has been rated among the Top 5 Semiconductor service companies in the USA by Silicon India.

Soctronics Inc.

Santa Clara, CA

www.soctronics.com

SoCtronics is a customer-focused VLSI design and embedded software service company operating since 2003. The company is headquartered in Hyderabad, India and has design center in Santa Clara, California. SoCtronics offers complete spec-to-silicon turnkey solutions that include embedded systems and software/firmware codevelopment. The company has over 500 employees world-wide and is privately owned and operated. For more information, please visit http://www.soctronics.com/.

Solido Design Automation Inc.

San Jose, CA

www.solidodesign.com

With technology rapidly going mobile, demand is increasing for high-performance, low power, low cost ICs. To create these chips, foundry processes are required which come at the cost of increased variability. Solido is a leading solution provider to de-risk these variation impacts, providing maximum yield at the performance edge for memory, standard cell, low power and analog/RF design. Solido's software solutions address the exponential analysis at 28/20nm and below without compromising time-to-market.

Sonnet Software, Inc.

N. Syracuse, NY

www.sonnetsoftware.com Booth: 2213

Sonnet Software provides high frequency electromagnetic (EM) software for 3D planar circuit and component model extraction. The Sonnet Suites are aimed at today's demanding design challenges involving predominantly planar circuits and antennas (including microstrip, stripline, coplanar waveguide, PCB (single and multiple layers) and RF packages incorporating any number of layers of metal traces embedded in stratified dielectric material. Sonnet integrates with most major EDA design flows. Visit our booth for information on Sonnet's latest software Release 13.

Space Codesign Systems Inc.

Montreal, QC, Canada

www.spacecodesign.com Booth: 417

Space Codesign's solution, called SpaceStudio, is advanced software for designing silicon chips that works at a higher level called ESL, or electronic system level. Using SpaceStudio to create their designs, engineers can rapidly evaluate hardware and software options, at the same time, in parallel, and achieve up to 30% reduction in product development time with improved quality.



10th Amissersony Albertion 2002 - 2012

Si2 Open Luncheon, A celebration of the 10th Anniversary of OpenAccess, Monday, June 4, Room 303, 12:15 - 1:30PM

Si2 Open Networking Reception, the Celebration continues! Monday, June 4, Room 301, 4:30 - 6:00PM

Registration for both events is free, register here: https://www.si2.org/openeda.si2.org/si2_store/#c1

Si2 Booth #1214



The **OpenAccess** standard API and reference database implementation is developed through the OpenAccess Coalition, an organization of the world's leaders in IC design.

WWW.si2.org



Booth: Lobby

Booth: 1030

Springer

New York, NY

www.springer.com

Get hands-on experience with Springer's multi-format publishing model: print - eBook - MyCopy (printed eBooks for \$24.95).

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SpringSoft, Inc.

Silver Exhibitor

San Jose, CA www.springsoft.com

SpringSoft is focused on delivering innovative technologies to address critical challenges in the development of complex digital, analog and mixed-signal designs. Our award-winning products enable engineers to speed debug, improve functional verification quality, and create optimal custom IC designs. Solutions include the 3rd-generation Verdi³™ Automated Debug Platform, Certitude™ Functional Qualification System, Laker™ Custom IC Design platform and ProtoLink Probe Visualizer.

StarNet Communications

Sunnyvale, CA

www.starnet.com

Booth: 1724 StarNet Enterprise takes remote access to Unix and Linux-based EDA tools to the next level up ... the Cloud.

Access EDA tools from Windows, Mac, Linux or iPad workstations by logging in through a browser.

StarNet Enterprise allows for load balancing between Unix hosts and advanced sessions sharing. Connections are secure, fast and persistent, meaning you can reconnect after losing connection to the remote host. Enterprise offers extensive IT admin features for setting up users, user groups and access permissions.

Symica

Kiev, Ukraine

www.symica.com

Booth: 702

Symica provides a suite of EDA tools for the analog and mixedsignal integrated circuit design. The suite includes schematic entry, SPICE simulation, mixed-signal simulation, and layout drawing. All Symica tools are integrated into and can be run from Symica Design Environment. Besides, Symica Design Environment integrates additional modules required for circuit design: Library manager, Schematic editor, Symbol editor, Hierarchy editor, Simulation environment, input/output translators, etc.

Synapse Design

San Jose, CA

www.synapse-da.com

Booth: 726

Synapse Design is the preferred design partner of many Fortune 500 System & Semiconductor companies around the world.

Founded in 2003, headquartered in San Jose with operations in Irvine, Boston, San Diego, Colorado, China, India and Europe. Synapse offers full turnkey solutions or deployment of large teams world-wide. We support our clients from architecture to GDS including analog IP and embedded software development.

We specialize in assisting our clients in developing their next generation ICs, across many product domains.

SYNAPTIC & TRAMS

Herley, DK

Booth: 1905

SYNAPTIC targets the optimization of manufacturability and the reduction of systematic variations in nanometer technologies through exploitation of regularity at the architectural, structural, and geometrical levels. Research efforts are focused on exploring and developing innovative design methodologies and EDA tools.

TRAMS targets the design of devices models for sub-16nm, bulk-CMOS, CNTFETs, FinFETs, III-V/Ge technologies including variability and aging mechanisms. It covers research on new compensating, tolerating and reconfiguration mechanisms to mitigate the variability effects at circuit and many-core system level.

Synopsys, Inc. - Corporate

🕻 Platinum Exhibitor 💃 Mountain View, CA

www.synopsys.com Booth: 1130,1730

For 25 years, Synopsys has provided the world's most innovative semiconductor companies with the EDA software, IP and services needed to meet increasingly complex SoC design challenges. Today, the world's leading semiconductor companies rely on Synopsys' comprehensive portfolio of integrated system-level, implementation, verification, IP, manufacturing and FPGA solutions to design their products more quickly and cost effectively with lower rick. Visit Synopsys at DAC or www.synopsys.com to loarn about risk. Visit Synopsys at DAC or www.synopsys.com to learn about the newest solutions available to help enable the next 25 years of

SynTest Technologies, Inc.

Sunnyvale, CA

www.syntest.com

Booth: 1408

Since 1990, SynTest has developed and commercialized many market-leading design-for-test (DFT) products, including Logic/Memory BIST (TurboBIST), Scan/ATPG (TurboScan), test compression (VirtualScan), and fault simulation (TurboFault). SynTest's DFT IP, e.g., at-speed scan/BIST, are silicon-proven accomplished by a rich particular of 384 protected. protected by a rich portfolio of 38+ patents. The TurboBIST-Logic product is used today by leading companies to reduce test-cost and improve quality. The newly released RobustScan product provides Framework for Logic and Memory Soft-Error Protection. SynTest tools are backed by the most dedicated support team.

SypherMedia International

Westminster, CA

www.smi.tv **Booth: 1009**

SMI is dedicated to development of turnkey technology products and services addressing today's security issues. SypherMedia Library (SML) is our camouflage technique applied to standard cell silicon libraries. SML is a unique and innovative technology that enables an ASIC design's own silicon to resist reverse-engineering attacks and provide anti-taper protection. SML utilizes standard tools and design methodology, doesn't rely on coatings or shields, and provides high return on investment for silicon manufacturers and customers using this technology.

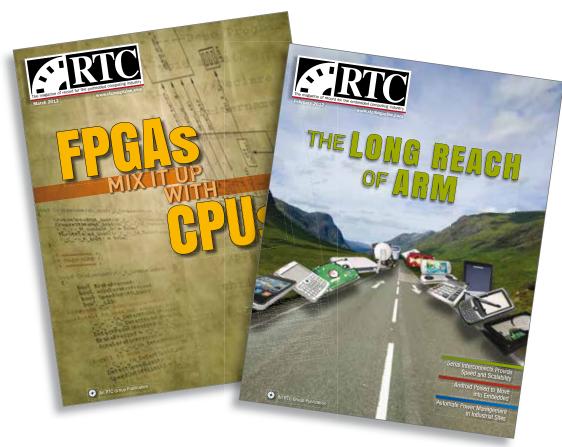
Tanner EDA

Monrovia, CA

www.tannereda.com **Booth: 1126**

Tanner EDA provides solutions that drive innovation for design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs). Customers are creating breakthrough applications in power management, displays and imaging, automotive, consumer electronics, and life sciences. A low learning curve, high interoperability, and powerful user interface improve design team productivity and enable low total-cost-of-ownership (TCO). Capability and performance are matched by low support requirements and an ecosystem of partners bringing advanced capabilities to A/MS designs.

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Target Compiler Technologies NV

Leuven, Belgium

www.retarget.com

Target is the leading provider of software tools for the design and programming of multicore SoCs using application-specific processor cores (ASIPs). Our ASIP design tools enable building of accelerators to offload standard CPUs, with performance and energy characteristics close to hardwired datapaths. Yet these accelerators provide software programmability, thus permitting changes in specifications and extending the revenue lifetime of the SoC. This year we also showcase our new multicore compilation tools, which help in parallelizing code for efficient load balancing.

Tektronix

Beaverton, OR

www.tektronix.com

Tektronix Embedded Instrument solutions greatly improve productivity for post-silicon validation of System on Chip (SoC) devices, ASIC prototypes and FPGA based system designs.

Tektronix is the market leader for bench-top instrumentation and are focused on delivering that expertise into the chip itself through a suite of products that address the need for access and diagnosis throughout the electronic product design process.

Tela Innovations

Los Gatos, CA

www.tela-inc.com

Booth: 704

Booth: 1001

Booth: 302

Booth: 826

Tela Innovations offers lithography optimized design solutions for advanced technology nodes eliminating the complexities of restricted design rules (RDRs). Tela offers physical libraries addressing the design challenges of RDRs, double patterning and FinFet from 32nm down to 14nm. Tela provides power optimization demonstrating significant reductions in leakage power on multiple production tape-outs from 90nm down to 28nm. This capability can be provided via design service engagements or by licensing the Tela Leakage Optimizer software tool. For more information visit www. tela-inc.com.

Tiempo

Montbonnot St Martin, France

www.tiempo-ic.com

Tiempo delivers an innovative approach to chip design platforms and design tools that leverage its patented clockless, delay insensitive technology. Its solutions address critical performance, security and PVT variation requirements in a wide range of applications.

Tiempo chip design relies on its breakthrough clockless design methodology using standard hardware description languages and ACC, its unique automated synthesis tool for clockless and delayinsensitive designs.

For more information, please visit www.tiempo-ic.com

TOOL Corp.

Tokyo, Japan

www.tool-corp.com Booth: 416, 612

TOOL Corp. will introduce LAVIS-plus, which extends and reinforces LAVIS functionality and performance, to further reduce your layout-to-maskout burden. LAVIS-plus maintains focus on interface to major commercial DRC/LVS products, miscellaneous tape-out functionality, failure analysis, a set of edit functions, and so on, propped up by a unique ultra-high performance engine. Moreover, LAVIS-plus adds user customization flexibility, smoother operations as well as performance brush-up to handle 20-nano-class data. So, come to our booth and experience this LAVIS-plus!

TowerJazz

Newport Beach, CA

www.towerjazz.com

TowerJazz provides design kits, IPs and dedicated design services for its process technologies for first-time working silicon and fast time-to-market. TowerJazz belongs to the IPL Alliance to deliver interoperability of process design kits (iPDKs) for its customers' analog/mixed-signal designs. TowerJazz has partnerships with every major EDA vendor and with IP providers to supply its customers with the most comprehensive and up-to-date design solutions and it has qualified reference flows for its 180nm power management process with several EDA vendors. www.towerjazz.com

True Circuits, Inc.

Los Altos, CA

www.truecircuits.com

True Circuits, Inc. (TCI) is the leading provider of timing IP for the semiconductor, systems and electronics industries. TCI develops robust state-of-the-art circuits using a methodical and proven design strategy and in close association with the world's leading fabs, IDMs and design service providers. TCI offers a complete family of high quality, low-jitter and standardized PLLs and DLLs in a range of frequencies, multiplication factors, sizes and functions in TSMC, GLOBALFOUNDRIES, UMC and Common Platform processes from 180nm to 28nm.

TSMC

San Jose, CA

www.tsmc.com

Booth: 2430

Booth: 1105

Booth: 2726

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry segment's largest portfolio of process-proven libraries, IPs, design tools and reference flows. The Company's managed capacity in 2011 totaled 13.22 million (8-inch equivalent) wafers, including capacity from three advanced 12-inch GIGAFAB™ facilities, four eight-inch fabs, one six-inch fab, as well as TSMC's wholly owned subsidiaries, WaferTech and TSMC China, and its joint venture fab, SSMC. TSMC is the first foundry to provide 28nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please visit http://www.tsmc.com.

TSSI - Test Systems Strategies, Inc.

Beaverton, OR

www.tessi.com

Booth: 703

Founded in 1979, TSSI is the world leader in design-to-test pattern conversion and validation software solutions.

Product engineering teams use TSSI VirtualTester (TVT) platform to migrate core-based patterns to chip-level and validate them by simply plug-in our ATE model to their DUT simulation environment to arrive at an ATE-ready pattern set pre-silicon, and achieve first time silicon bring-up success.

Visit our booth to see how TSSI's customers shrink their silicon bringup time from months to hours.

TSSI – We bring "Test to Design".



Perfect timing requires speed and precision, particularly in the noisy universe of digital chips...

True Circuits offers a complete family of standardized **PLL** and **DLL** hard macros that have been specifically designed to meet the precise timing requirements of the latest DDR, SerDes, video and other interface standards.

These **PLLs** and **DLLs** are available for delivery in a range of frequencies, multiplication factors, sizes and functions in TSMC, GLOBALFOUNDRIES, UMC and Common Platform processes from 180nm to 28nm.

Rise above the noise. Lock in a premium-quality, low-jitter **PLL** or **DLL** that you can count on for first silicon success.



Speed

Wide output frequency ranges Large multiplication factors (1-4096) GHz frequencies for Gb/s data rates



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Tyndall National Institute DTE Group

Cork, Ireland

www.tyndall.ie/DTE

Booth: 309

Booth: 1008

Booth: 1902

The Tyndall Institute has over 400 staff and over €180 Million of laboratory infrastructure and specialises in Micro/Nano Electronics. Photonics, Microsystems, Theory Modelling and Design.

Within the US and Europe, Tyndall's DTE group provides professional measurement and analysis services to IC designers and process technology developers, as well as the IP assertion community. We specialise in:

- intellectual property, copyright and counterfeit investigation.
- electrical design evaluation and diagnostic measurements.
- assessment of IC designs and technologies.
- FPGA systems design.
- LabVIEW© & embedded software development.

UMIC Research Centre

Aachen, Germany

www.umic.rwth-aachen.de

UMIC is a research cluster focusing on the demands of future mobile applications and systems. Activities cover research on basics concepts and new paradigms, the development of tools, prototypes and demonstrators, and the technology transfer to industry.

At DAC'12 high-level synthesis flow based on Architecture Description Language will be presented. It converts algorithm description in C code into ASIC model and is captured in LISA representation. This facilitates the design space exploration ranging from high-performance ASIC to highly programmable ASIP.

Uniquify, Inc.

Santa Clara, CA

www.uniquify.com

Uniquify provides ASIC/SSoC design services, SSoC integration and manufacturing services, and high performance IP to a broad base of customers including fabless semiconductor companies, system manufacturers, foundries, and IDMs. Our Perseus™ ASIC/ SSoC design management frame work enables us to deliver fast, repeatable and consistent complex SSoC design closure. By combining our design expertise and manufacturing services with our IP portfolio, we offer a complete "turnkey" solution that spans chip specification and design through the volume delivery of packaged and tested parts. Please stop by and visit us at Booth.

Univa

Hoffman Estates, IL

www.univa.com

Booth: 1503 Univa, the Data Center Automation Company, is the leading provider of automation and management software for computational and big data infrastructures. Our products and global enterprise support give our customers the ability to manage their entire computational space, no matter how big or where it is deployed. Many of the worlds leading brands depend on Univa's unsurpassed knowledge, expertise and support. Univa is headquartered in Hoffman Estates Illinois and has offices in Markham Ontario, Austin Texas and Munich Germany.

Vavavva Labs Inc.

Santa Clara, CA

www.vayavyalabs.com

Vayavya Labs provides leading edge solutions that accelerate embedded software and firmware development. The patented device driver generation technology provides a 10x productivity boost by synthesizing driver code from specs, thereby enabling silicon providers and system vendors to ensure timely delivery of the necessary OS ports and BSP's to their customers. The programmatic spec capture can also be leveraged to define a common pre-silicon to post-silicon validation methodology which helps streamline verification, thereby lowering R&D cost.

Vennsa Technologies, Inc.

Saratoga, CA

www.vennsa.com

Booth: 1901

Booth: 710

Vennsa's OnPoint™ is the industry's only automated debugging tool that localizes the source of errors with absolutely no user guidance. OnPoint eliminates today's time consuming manual debugging of RTL failures that takes more than half of the verification effort. OnPoint automatically points engineers to the root cause of failures and suggests how to fix the bugs. OnPoint's technology picks up where verification tools leave off, saving weeks or months of effort while guaranteeing faster design closure to dramatically improve productivity.

Verific Design Automation

Alameda, CA

www.verific.com

Booth: 1807

Verific Design Automation provides the (System) Verilog and VHDL front-ends for a majority of EDA and FPGA tools. When you are parsing RTL, the software is likely to come from Verific. And more and more semiconductor companies are joining they fray as they use Verific's Perl APIs to build their own one-of-a-kind (System) Verilog and VHDL flows with Verific. More than 60 corporations worldwide are now using Verific. Isn't it time you gave it a try?

Verification Academy

Wilsonville, OR

www.verificationacademy.com

The Verification Academy is the most comprehensive resource available for verification training. Organized into a collection of free online courses, resources and forums, the Verification Academy focuses on key aspects of advanced functional verification, including: UVM/OVM, Assertion-Based Verification, Verification Management, CDC Verification, Acceleration, FPGA Verification, Intelligent TB Automation, and more. Join us in the Verification Academy Booth for user and partner presentations, UVM applications, daily technical discussions with Harry Foster and other prominent Verification experts and our Tuesday cocktail reception.

Veritools, Inc.

Los Altos, CA

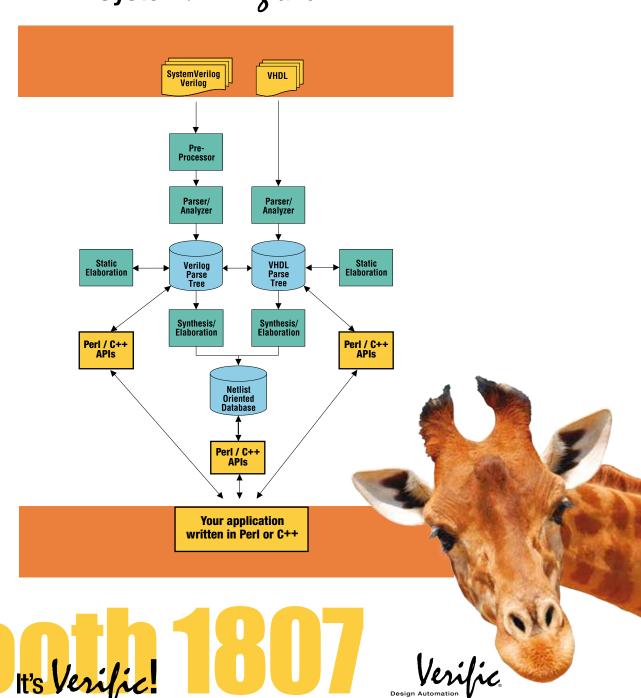
www.veritools.com

Booth: 1823

Veritools offers powerful RTL Verilog/SystemVerilog/VHDL source code debugging and waveform display software. VeritoolsDesigner UT2K12.1.0, which when integrated with a built in SystemVerilog is VeritoolsVerifyer. This SystemVerilog Assertion simulator Assertion simulator speeds up design verification by 100s of times verses a standard Verilog/VHDL/SystemVerilog simulator. Features include a high speed ULTRA mode, for 3-12 X faster waveform viewing with analog and digital designs, and software for computing HSPICE measures in batch mode, eliminating re-simulation.

Build your own RTL tools!

with Verific's development platform for System Verilog and VHDL



Booth: 1114

Booth: 730

Booth: 600

Booth: 1115

WinterLogic Inc.

Roseville, MN

www.winterlogic.com

WinterLogic's functional fault simulator, Z01X, is used by companies that demand the highest level of quality, including many of the world's leading high volume consumer, automotive microcontroller and security IC manufacturers. Our expert test system helps companies hit their zero-defect target by selecting the most effective functional tests, reducing tester time, and closing the ATPG coverage gap. In addition, Z01X's new verification assurance feature aids in verification closure by combining controllability and observability to identify untested and unobserved RTL code, providing true test coverage.

Xilinx Inc.

San Jose, CA

www.xilinx.com

Xilinx (NASDAQ: XLNX) develops All Programmable technologies and devices, beyond hardware to software, digital to analog, and single to multiple die in 3D ICs. These industry leading devices are coupled with a next-generation design environment and IP to serve a broad range of customer needs, from programmable logic to programmable systems integration. For more information, visit www.xilinx.com.

XYALIS

Grenoble, France

www.xyalis.com

XYALIS presents GTmodus, an enterprise-wide mask data management system, providing semiconductor companies with an error-free, 100% SEMI-P10 compliant mask order process warranting interoperability between mask suppliers, complementing the most advanced fully automated Mask Data Preparation suite on the market.

XYALIS also offers an advanced CMP metal fill solution, optimizing accuracy and runtime while minimizing impact of dummy tile insertion on performance and memory usage, that has been successfully used on a multi-billion transistor processor design using TSMC 28nm process.

Z Circuit Automation

Mountain View. CA

www.z-circuit.com

Z CIRCUIT is an EDA company offering advanced circuit analysis and cell library development software products including ZCHAR LIBRARY CHARACTERIZATION, ZCHAR MEMORY CHARACTERIZATION, and LIBRARY ANALYZER.

ZCHAR is a sophisticated all-in-one system for cell library characterization of standard cell, memory, IO pad, and custom cells. LIBRARY ANALYZER is the industry-leading tool for library validation, corner consistency checks and analysis for any cell libraries.

New this year is our second-generation standard cell product, crossview checker, ultrafast memory characterization and advanced low-power cell models.

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IROC Technologies Corp.

Mountain View, CA

www.iroctech.com

IROC Technologies significantly lowers the risk of radiation-induced failure for integrated circuits (IC) throughout a product's lifetime, by design optimization. The company provides designers with soft error prediction software, test services and expert advisors to improve IC reliability. Companies using TFIT® and SOCFIT® software need high performance and high reliability in application areas such as cloud infrastructure, Internet infrastructure, automotive, medical devices and aerospace. IROC's U.S. headquarters are in Silicon Valley, California, European headquarters are in Grenoble, France.

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San Jose, CA

www.arm.com

ARM designs the technology at the heart of advanced digital products, from wireless, networking and consumer entertainment solutions to imaging, automotive, security and storage devices. ARM's comprehensive product offering includes 32-bit / 64-bit RISC microprocessors, graphics processors, video engines, logic libraries, embedded memories, and high-speed connectivity products.

The ARM® Artisan® physical IP platforms deliver optimized IP for best-in-class processor implementations on GLOBALFOUNDRIES manufacturing processes. These platforms are comprised of easy-to-use logic libraries, memory compilers and interface IP offering System-on-Chip (SoC) designers the ability to balance performance, power, and area for optimal SoC designs and reduced time-to-market.

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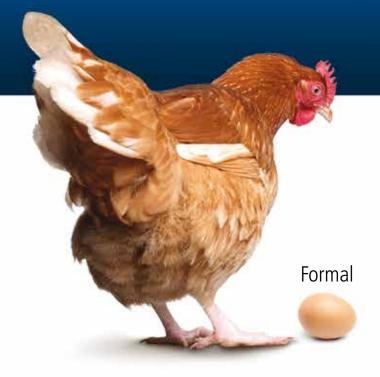
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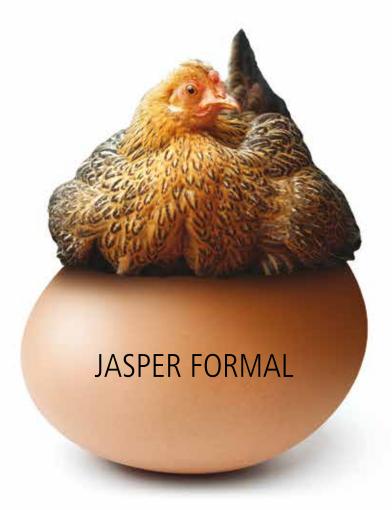
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