Session Title	Session Description	Submission Title	Contributors
AI and Chiplet/Multi-die: Verification Scalability and AI driven Automation	Chiplet based design demands scalability and AI can provide multifold gains in productivity by automating flows and providing new solutions. In this session, presenters will share their insights into flows/methodology for Chiplet based design and how AI can be leveraged to transform the verification landscape.	Enhancing verification throughput in random tests regression with a novel machine learning engine	Davide Sanalitro
		An Automated and Scalable Monitor-and-Checker solution for SMMU verification in Multi-Die SoCs	Junha Jeon, Namyoung Kim, Hyunman Park, Jaein Hong, Moonki Jun, Sanghune Park
		A Leap Forward in Formal Verification Using Generative AI	Shahid Ikram, Sean Safarpour, Alex Chang
		Revolutionizing Digital ASIC Design through AI	Paulo Magno, Ricardo Araujo, Miguel Caetano, Mara Carvalho, Luis Cruz, Luis Francisco
		Expediting UCIe and Boot Verification using Distributed Ndie Simulations and Emulation for Multi-Chiplet AI SoCs	Harshal Kothari, Jerin Jose, Jasobanta Sahoo, Ayush Agrawal, Madhukar Ramegowda
		Fear Not! With LLMs, Learning PSS Isn't Scary At All	Tom Fitzpatrick, Mohamed Moselhy, Sarah Heshmat, Mohamed Nafea, Waseem Hasan, Dan Yu
Arrival Pathways for Crossing the Chip-n-Package Routes	Learn the routing strategies to cross the maze of chip to packaged parts delivery - keeping the clocks aligned to finding ways around crowded area or feeding throughs that cut the walls. Get Set and GO!	Dynamic Optimization of Skew Balancing through an Innovative Correct-by-Construct Path Delay Query Technique	Tejas Salunkhe, Subhadeep Aich, Abhranil Bose
		Routing Congestion Mitigation Techniques Targeting Dense Designs	nancy Zhou, Lakshmi Reddy, Alex Suess, Bijian Chen, Nathaniel Hieter
		ML based PPA Push using XAI	Kyoungsun Cho, Mintae Lee, jungho kim, Sungyoul Seo, Kibum Nam, Bonghyun Lee, Ki-Ok Kim
		Efficient Automation Strategy for Package Substrate Routing	Keng Tuan Chang, Chih Yi Huang, Chen Chao Wang, Chin Pin Hung, Woei Haur Hung, Ting-Chi Wang
		A Novel Feedthrough Insertion Methodology for Hierarchical SOC Designs: Achieving Reduction in Die Area	Rajanikant Sakariya, Subhadeep Aich, Vivek Joshi, Roger Griesmer
Back-end and System Considerations for Chiplets	Join us for a comprehensive session that explores the latest advancements in chiplet integration and 3DIC design, focusing on security, optimization, and thermal management, offering valuable insights into cutting-edge methodologies that enhance the reliability, efficiency, and performance of modern SoC and 3DIC systems. We start with a deep dive into secure chiplet integration within System-in-Package (SiP) architectures, detailing methods for secure authentication, remote	SuperCoverage: AI-Guided Full Coverage of Thermal and Power Analysis for SoC Design	Xia Zhu, Jianfang Zhu, Mark Gallina, Julien Sebot
		High Performance Extraction of 2.5D/3D-IC Package	Xiaoyan Xiong, Yingxin Sun, Jiyue Zhu, Gang Kang, Jian Liu
		Accurate Thermal Simulation of 3DIC Package with Co-Packaged Optics	Ahsan Alam, Qinglian Li, Lucy Yin, Lang Lin, Wenbo Xia
		Analysis of Electrostatic Discharge (ESD) for 3DIC systems	Anila Azam
		Securing Chiplet Integration: A System-in-Package Security Architecture.	Sylvain Guilley, Junie Um
Complete Your Power and Thermal Envelopes with Security and Predictability	Keep your cool while removing heat and not revealing your secrets to performance and security. This season deliver secure designs that don't melt down.	A Hybrid Simulation Technique for High-Speed and Accurate System-Level Side-Channel Leakage Analysis	Kazuki Monta, Takafumi Oki, Rikuu Hasegawa, Takuya Wadatsumi, Takuji Miki, Makoto Nagata, Lang Lin, Norman Chang
		PPA Evaluation of BS-PDN Compared to FS-PDN in the Early Stage	Dean Huang, Andy Wei, Chee How Lim, Yi-Wei Chen
		Mitigation of Functional Power Dissipation in Parasitic Scan Shift Test Buffers	Aradhana Kumari, Ankur Bal
		A Simulation Technique of Thermal Side-Channels from Cryptographic Circuits	Shuhei Yokota, Rikuu Hasegawa, Kazuki Monta, Takaaki Okidono, Takuji Miki, Makoto Nagata
		3DIC Thermal-Aware Early Design Optimization	Chia-Yi Liou, Chih-Hsiang Yang, Kuan-Ting Kuo, Chung-Ching Peng, Venkatesh Ramamurthy, Vivek Rajan, Narender Akilla, Naresh Mummidivarapu, Yashodhara Tarey, Kumar Subramani, Yi Wei Chen
Custom IP Blocks – The Lego Blocks of Digital Design	Hardened IP blocks, from the humble inverter to the multimillion transistor SRAM macro, are the basis without which digital design cannot exist. Creating, extracting and characterizing them is therefore a crucial step in their generation flow. This session describes techniques for the design and view generation of hard IP that help achieve the optimal PPA results.	Logic and SRAM Library Generation and Analysis for Digital Design Enablement	Sravanth Mucharla, Shruti Rakheja, Ray Valencia, Shane Toma
		An engineering approach to high performance scannable flip flops embedding functional logics	Min-su Kim, Yong geol Kim, Daeseong Lee, Hyoungwook Lee
		Robust Verification for Complex Liberty IP	Ray Valencia, Ajay Kumar, Santhosh Kamatam, Khushboo Rathore, Pramod Gayakwad
		Scenario-based Mixed Signal Layout Generator using Generation APIs for Memory	Jeongyoon Lee, Kyeongrok Jo, Seungkwang Hong, Sichan Kim, Seunghwan Lee, Youngwook Kim, Jungyun Choi
		Novel IC layout parasitics analysis techniques to enhance Custom Macro/IP and Standard cell library development flow	Ravi J N, Kopal Kulshreshtha, Pramod Gayakwad, Maxim Ershov, Santhosh Kamatam
Formal and Static Verification: Stop Bugs Before They Think They're Invited	Static and formal based flows/solutions provide a bottom-up verification approach, helping engineers find certain class of bugs in the shortest time and helping manage efficient distribution of load across all verification technologies. In this session, presenters will share their experiences on applications like data path validation, formal verification, and metastability analysis (CDC/RDC).	Formal Property Verification on Xeon SoC owned IPs	Prakeerthi Jallipalli
		Identifying Soft-Resets in Design using RDC Tool Flow	Megha Hansaliya, Sushovan Kunti
		Formal signoff for Cross-Module Design logic: A novel approach to manage formal scope in increasingly complex systems	Sai Asrith Tabdil, Sakthivel Ramaiah, Clarice Oliveira, Sorna Inian
		Taming Formal to define the Verification Quality	surinder sood, kishan mushar
From Devices to Debug - Modeling Thoughtful Design Practices	Learn from the smorgasboard skillset needed to dive deep into the world of devices to working devices that deliver impactful semiconductors cost effectively - from transistor devices, PDK and models to debugging parts and interconnect design	Enhancing PDK Library Validation with Machine Learning. A Novel Approach to Layout Comparison	Nolan Pavek, Romain Feuillette, Farzana Akhter
		Machine Learning (ML) Assisted IBIS-AMI Model for Optical Module Involved Advanced SerDes System Designs	Ruoshi Xu, Zeqin Lu, Xinying Wang, Curtis Clark, Saeed Asgari, Wei-hsing Huang, Bozidar Novakovic, Dylan McGuire
		A novel structure to achieve broadcastable IJTAG network	Feilong Pan, Minqiang Peng, Lei Yang, Keqing Ouyang, Guohua Zhou
		Recalibration of MOSFET Compact Models based on Complex Product-Related Layouts using Bayesian Optimization	Lan Luo, David Winston, Robert Perricone, Bria Matthews, Richard Wachnik
		Generation of Failure Inspection Pattern without Design Impact during P&R in BSPDN Design	Woojin Jin, Sangun Park, Joowan Lee, Haemin Yoo, TaeYang YOU
Grid Resilience - Powering Solutions Design and Delivery for the Performance Promises	Power keeps the engine humming and delivering promised performance. Learn from others that have modeled power delivery early to signoff and doing it smart - Multi-die to ML driven with an eye for analytical speed is the focus of this session.	Generative-AI Technology for block and SoC IR closure: Root-Cause and Repair strategies	Jaikishan Gopal, Siki Yang, Shane Gallagher, Sandhya Karanam, Keith Tunstall, Rohit Somwanshi, Jinal Apte
		Machine Learning based Dynamic IR hotspot estimation for SoC Designs	Prateek Pendyala, Jingwei Zhang, T Govindaswamy Rahul Sai
		Comprehensive Power Integrity Analysis of a Super Large Scale 2.5DIC with Multi Silicon Bridges Embedded in Organic Interposer	Ping Ding, Guohua Zhou, Shineng Ma, Li Zou, ShuQiang Zhang
		Guided Vectorless with Multi vector profiling for Memory PDN convergence	Alina Sebastian, Mohammed Hafiz
		IR Drop-Aware PDN Design Methodology for HBM Proxy Package Si-Interposer with 3D-IC Platform	Youngho Seo, Gwonhyuk Kang, Sangwon Lee, Kun Joo, Donghwi Won, Juhwan Lee, Jinwon Kim, Jungyun Choi, Youngsoo Sohn
IP Gold – New Digital Design Nuggets	This session presents six interesting digital IP components and design techniques. It covers resilience against side channel attacks in encryption IP as well as new blocks addressing the need for communication protocols, low power clocks, decimation cores and vector floating point math units.	Energy Efficient I3C IP Subsystem for Low Power IoT	Aradhana Kumari
		Simulation-based Pre-Silicon Side-Channel Analysis of AES-GCM	Emrah Karagoz, Karthik Gedela, Ferhat Yaman, Amitabh Das, Sourabh Goyal
		Balancing Performance and Side-Channel Resilience in a Lightweight ECC Cryptosystem	Harikrishnan Balagopal, Lang Lin, Norman Chang, Mitra Mirhassani, Seyedeh Nejati
		Hybrid and Adaptive Digital Filter architecture for Robust tracking of On-chip Low Frequency Oscillator Period, enabling Crystal less BLE operation in Low Power Wireless MCUs	Anurag Choudhury, Robin Hoel, Torjus Kallerud, Ashutosh Mishra
		Reconfigurable Vector Floating Point Accelerator on FPGAs	Himanshu Rai, Sasi Snigdha Yadavalli, Aishwarya Sridhar, Nanditha Rao

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Novel Eddies in the Implementation Flow	A consistent and streamlined implementation flow is key for combining IP blocks into a working SoC and ensuring correct operation. This session presents new approaches for timing closure, meso-synchronous clock domains, high level synthesis, modeling of clocks and reset, randomizing memory content and managing large sets of simulation jobs.	A Completely Digital, Low-Power, and Low-Area Phase Synchronization Architecture for Meso-Synchronous Clock Domains Supporting Dynamic Frequency Scaling	Anurag Choudhury, Robin Hoel, Aniruddha N, Abhishek Verma, Abhinav Parashar
		A novel approach to generate random/constrained Non-Volatile-Memory content in a UVM environment	Davide Sanalitro
		Optimized Digital Design Flow for Embedded Sensor Applications Using High Level Synthesis	Marco Castellano, Ugo Garozzo
		AI-aided flow for digital verification of a multiprotocol SerDes PHY	Celso Figueiredo, Domingos Terra
		Cross-die timing methodology for Next-Gen Chiplet SOCs - A shift-left solution for cross-foundry 3DIC-STA Signoff	Deepon Saha, Animesh Sharma, Animesh Jain, Aniket Waghide, Dhruvin Shah, Rajesh Anand
Software Development & AI Applications	This session delves into cutting-edge methodologies and frameworks revolutionizing system-on-chip (SoC) development, software optimization, and artificial intelligence collaboration. Explore advanced hybrid emulation techniques that accelerate Android home screen bring-up and system software validation at the pre-silicon stage, reducing time-to-market and debugging complexities. Discover innovative power-saving strategies for	Rom-based automotive boot code, in compliancy with functional safety and cybersecurity standards	bipul halder, Davide Fiorese, Neha Saxena, Agata Notario, Simone Colle
		Flexible Integration of a Neural Network Library in TensorFlow Lite Framework for Efficient Programmable Near-Memory Computing Architectures	Maha Kooli, Thaddée Bricout, Jean-Philippe Noel, Henri-Pierre CHARLES, Maria Ramirez Corrales
		TrustChain: Enabling Consensus-Driven Multitasking AI	Arpita Sarker
		Accelerated SoC Level Android Home Screen Bring-up, System Software Development and Validation at Pre-Silicon with Advanced Hybrid Emulation Methodology	Rinkesh Yadav, Sarang Kalbande, Naushad Kollikkara, Garima Srivastava, Hyundon Kim
Surviving Monte Carlo – Circuit Optimization Ideas	Analog circuits are difficult to optimize and traditionally require a large number of Spice level simulations to determine performance and sensitivities. This session presents new ideas that employ AI or other methods to facilitate this task.	Statistical analysis using AI-ML enabled SPICE solution to get tail samples for high linearity delta sigma converters	Vaibhav Garg, Sanyam Jain, Atul Bhargava, Ankur Bal, Anil Dwivedi, Prayes Jain
		Advanced Verification Solutions for Communication ICs to Ensure High Quality Amid PVT Variations	Tomohiro Ishida, Shunichi Kobo, Yuling Lin, Lih-Jen Hou
		Accelerating Bandgap Reference High-Sigma Verification with Additive AI Technology	Barry Thompson, Lawrence Prather, Mohamed Atoua, Hadar Baran, Kevin Krieger
		AI-Driven Multi-Parameters Multi-Objectives Optimization Flow For High-Speed Transmission Line In SerDes Design	Long Qin, JinRong Yan, Dengjie Wang, Hang Sun, Xuewei Ding, Xiaomei You, Rodger Luo, Jie Cheng
		Accelerating SRAM Design Cycles With Additive AI Technology	Mohamed Atoua, Ajaj Ansari, Sriharsha Enjapuri
		Novel TRNG Verification with a High-Performance Simulation Methodology	Ting-Yen Chiang, Shravan Ramesh, Lih-Jen Hou
Verification Innovation: Shaping the Future of Design Validation	Join us to learn about new strategies in the catch-up game verification engineers play daily with the increasing design complexity and tighter schedules. In this session, presenters will talk about advanced verification techniques spanning from RTL to GLS covering Python, UVM and SystemC driven solutions.	Enhancing Verification Efficiency with Garbage-Model Methodology	Stas Yosupov, Smadar Eliyahu-Shulemzon
		Refresh your UVM Testbench with a Spritz of Python	Matthew Ballance
		AUTOLNKGEN: Automated Random Linker File Generation Framework for Heterogenous SoC Verification & Validation	Mohan Udayakumar, Yogeshwaran Shanmugam, Suraj Salian, Rakesh YC, Aswin B
		Netlist Powered Emulation Paradigm: Pioneering Breakthroughs in Gate Level Verification	Samhith Pottem, Vasudeva Reddy, Jaesung Park, Sarang Kalbande, Garima Srivastava, Hyundon Kim
		AACT: Automated Analog Coverage Tool for Mixed Signal Verification	Bhavya Shah, Aadhar Sharma, Gayathri M, Avinash Chaudhary, Atul Lele
Watt's Next: Low-Power Design and Verification Trends	Accurate power analysis is crucial for designing power-optimized silicon, especially as modern applications demand higher performance within stringent power and thermal constraints. In this session, presenters will share their experiences and insights into advanced power analysis techniques and optimization strategies across a wide range of applications.	A Novel approach for workload based GPU datapath power optimization	Deepayan Dasgupta, Tanuj Sengupta
		Enhancing RTL Power Accuracy with Advanced Buffer Modeling for Improved Efficiency and Correlation	Fengyu Xiao, Shixuan Que, Sai Li, Lei Bao, Ling Sun, Zhongming Hou, Zhenbang Wang
		Unveiling the Core Truth: Advanced Glitch Power Analysis and Optimization Using Statistical Methodology	chenyang Zhang, Zhongming Hou, chen lin, Jinbo zhu, Yuchao Liu, chao Gu
		Streamlining Low Power Verification for Multi-die SoCs: A Comprehensive Framework	Jaein Hong, Junha Jeon, Yujin Oh, Moonki Jun, Sanghune Park
		Optimal Power Estimation Methodology for CXL Memory Controllers	kyeongseob kim