



Session Event Types	Session Title	Session Description	Submission Title	Contributors
Back-End Design	Electron Signatures for Predicting the Diagnosis	Enhance your work to identify the signatures underlying high bandwidth interfaces, chip package board co-design or just closing optical and silicon robustness from leaking secrets to the outside world.	Die, Package and PCB Co-design for Low Area, High Signal to Power Pin Ratio in High Frequency SOC designs	Karthik Kodakandla, Jakeerali Shaik, MuraliMohan Thota
			Si Backside Side-Channel Leakage and Simulation of Cryptographic IC Chips	Rikuu Hasegawa, Kazuki Monta, Takuya Wadatsumi, Takuji Miki, Makoto Nagata, Lang Lin, Sreeja Chowdhury, Akhilesh Kumar, Norman Chang
			Pre-Silicon Photon Emission Modeling and Optical Side-Channel Simulation	Henian Li, Lang Lin, Norman Chang, Sreeja Chowdhury, Kazuki Monta, Makoto Nagata, Mark Tehranipoor
Back-End Design	Explore Concepts of STA Thru Insightful Craftsmanship	Explore how you drive STA through 3D to ML techniques or simply closing timing on large designs be it through pruning margins, multiple clock sources or just partitioning effectively.	TSV KOZ separation 3DIC P&R area optimization methodology considering device impact by TSV	Yongjin Hong, Ki-Ok Kim, Mijeong Lim, Jun Seomun, Byunghyun Lee, Sangyun Kim
			ML based PPA Push using DRV Prediction	jungho kim, kyoungsun cho, sunghoon kim, Mintae Lee, wook kim, Ki-Ok Kim, sangyun kim
			Pruning Netlist: A Smarter Approach to Efficient and Reliable Circuit Characterization	Harsh Garg, Pawan Verma, Saurabh Srivastava, Anil Dwivedi, Fillaud Matthieu
			Clock parameter tuning with an intelligent adaptive learning to improve performance and power of Multisource Clock Tree Synthesis	Divyarajsinh Vaghela, Jagadeesh Gnanasekaran, Gaurav Bhatia
			An effective Hierarchical STA solution for closing Large SoC Design	Shourya Shukla, Sushant Hajare, Sainarayanan Suryanarayanan, Harshit Jaiswal, Sharath AC, Nitin Jain
Back-End Design	Exploring Alternative Corridors for Optimal Routes	Find your inner Nemo! Explore multiple pathways to getting around the barriers in floorplanning, be it memories, cutlines or using the symmetry of the edges. Use AI to assist your route plan.	A Novel Solution for Fast and Efficient Custom Bus Routing with User-defined Reference Wire and Combination of Segmented Bus Option	SUNGSIK PARK, Keunbong Lee
			Memory IO Block Routing Optimization using Semi-Automation of Single Trunk Steiner Tree Routing	Seyong Ahn, Hyeyoun Kim, Kwangok Jeong, Jungyun Choi
			A New Frontier for Floorplanning with AI	Pinkesh Shah, Alpesh Kothari, Raghu Ram Gude
			Automatic Layout Symmetry Annotation via Graph Node Embeddings	Jerome Lescot, Francois Lemery
			High Confidence Hierarchical bottom-up DVD methodology for EMIR Signoff of Automotive SOCs	Love Gupta, Manmeet Singh, Koshy John
Back-End Design	History, Present, and Future of STA: A Travel Through Timing	Static Timing Analysis (STA) has evolved dramatically in the last 20 years. From a fairly simple extraction and back annotation of a single flat entity, and analysis in a couple of bounding timing corners, it has grown exponentially as technology nodes have advanced to consider many other physical factors, and handle design data sizes and STA engineering team sizes almost unthinkable 20 years ago. Join us on this historical retrospective, a brief check-in to current STA techniques and requirements, and a glimpse into the future as to what may be coming in the near future, and what EDA can do to help. Speakers from Marvell, Synopsys, and IBM will cover the full history, present and future of STA in this exciting and entertaining presentation.	History, Present, and Future of STA: A Travel Through Timing	Bertram Bradley, Sabya Das, Tim Helvey, Peivand Tehrani, Kerim Kalafala
Back-End Design	Thermo-Electrical Analysis and Signoff Engagement	Deliver a successful solution teaser by learning about ways to model the double helix of thermo-electric impacts on system design closure for timing, power supply delivery and test	Efficient representation of cross current effects in contributor-based power models	Spandana R, Arun Joseph, Nagu Dhanwada, Rahul Rao
			Timing Robustness: A Way forward for analyzing timing-voltage sensitive paths for accounting IR-Drop Variations	Shourya Shukla, Lavanya Padmanabhuni, Sainarayanan Suryanarayanan, Harshit Jaiswal, Sharath AC, Nitin Jain
			Automated Workflow for Comprehensive Thermal Analysis of IC Package Designs	Sharath C R, Senthil Kumar Sundaramoorthy, Siva Gurrum, Blake Travis
Embedded Systems and Software	Embedded Systems and Software	Embedded Software is a critical differentiator in today's designs, and its close relationship with hardware aspects specifically impacts hardware/software flows and development methodologies. This session will discuss aspects like accuracy enhancements for virtualization to enable early software development, system design aspects of power, firmware verification, reinforcement learning for test optimization, automotive AUTOSAR software aspects, and mapping challenges of software to computing resources.	No-Code Power and Clock System Design	Hoyeon Jeon, Ahchan Kim, Ingyu Kim, Jongbae Lee
			Functional Accuracy Enhancement of In-House Virtual Platform using Commercial IP Model	Jooho Wang, Dongyoung Lee, Myeongjin Kim, Sangwoo Han, Seungik Ha, Jinbeom Kim, Jaeyeong Jeon, Songyi Park, Jongseong Park, Kyungsu Kang, Jaewoo Im
			Complex application mapping to heterogeneous compute resources	Wesley Skeffington, Surya Chongala, Deepak Shankar
			Automated Generation of SSD Stress Tests Using Offline Reinforcement Learning	Sunghye Lee
Front-End Design	Advanced Verification	Join us to learn about new strategies in the catch-up game verification engineers play daily	Use UVM for AMS DFT through IEEE 1687 Procedural Description Language	Hitu Sharma, Geert Seuren, Rahul Lodwal



Session Event Types	Session Title	Session Description	Submission Title	Contributors
		with the increasing design complexity and tighter schedules. In this session, presenters will share their wisdom across HLS, FuSa and hardware/software verification.	Shift Left with Improved Power-Awareness in RTL Stage Design for Early Design Verification	Penchalkumar Gajula, Lakshmanan Balasubramanian, Gaurav Varshney, Sooraj Sekhar, Siddharth Sarin, Ruchi Shankar, Nikhita Gorja, Nikhil Kumar
			Enhancing Quality and Reducing Verification Effort for RTL Implementations against High-Level C/C++ Models using Formal Equivalence	David Vincenzoni, Gianluca Rigano, Gaetano Raia, Maurizio Martina
			A Distributed Co-Simulation Environment and its Application in HW-FW Verification	Nitin Pundir, Pretty Jacob, Arun Joseph, Viresh Paruthi, Sandeep Korrapati, Ali El-Zein, Zoltan Hidvegi, Bodo Hoppe
Front-End Design	Industry Trends in the Front End	Emergence of AI has fueled an arms race to design new kinds of hardware to run them optimally and that in turn is accelerating innovation in design and verification methodologies. Come and learn the latest industry trends in front-end design, from Co-pilots in design and verification to improving PPA using AI.	AI-Powered High-Sigma Automated Full Library Verification Methodology for Standard Cells	Chengcheng Liu, Mohamed Atoua
			Shift Left Detection and Root Cause Analysis of Synthesis Optimized Registers at RTL Level	Sathappan Palaniappan, Kartik Agarwal, Himanshu Kathuria, Jaskaran Ajimal, Amit Jalota, Harsha Somashekar
			Design Constraint Strategy For Dealing With Cascaded Clock MUX Structures	Anish Keshava, Aakarshak Nandwani, Nitesh S, Satyanarayana Patnala, Sridharr S
Front-End Design	Static and Formal Verification: Pillars of Modern Design Assurance	Static and formal based flows/solutions provide bottom-up verification approach, this helps to find certain class of bugs in the shortest time and help manage efficient distribution of load across all verification technologies. In this session, presenters will share their experiences on applications like data path validation, formal verification, and CDC (clock domain crossing) verification.	Enhancing Formal Equivalence for Datapath Algorithms: A Proof Strategy with Intermediate Modeling to Address Structural Differences in Implementations	Suraj Kamble, Swaresh Phadke, Disha Puri, Aarti Gupta
			Leveraging Formal Verification to Create, Reproduce, Verify Design Scenarios from Simulation Wave-dump	Ujjwal Talati, Saikiran Ashwini, Aman Chauhan, Viraj Rawal, Nivin George
			Formal CDC Glitch Check - Advanced Sign Off Solution	Noam Eshel Goldman, Liad Nehama, Vikas Sachdeva, Polina Pashayev
			Breaking the Formal Convergence Barriers of a Floating-Point Dot-Product Block for AI/ML Accelerators	Satyabrata Sarangi, Neelabja Dutta, Sai Ma, Ashish Kapoor, Reily Jacoby, Adrian Lewis, Rohan Mallia, Eda Sahin
			Securing Safe Customization of RISC-V Cores via Rigorous Sequential RTL Comparison	Nicolae Tusinschi, Laurent Arditi
			A novel formal verification technique to System verification using contract refinement	surinder sood, Nirmal Jose, Scott Meeth
IP	Advances in Mixed Signal IP Design	Design automation has been the holy grail of mixed signal analog design. Unlike digital P&R design, mixed signal design has many challenges to overcome for automation and efficiency. In this section we present a collection of papers that improve simulation, test, and validation using AI/ML techniques.	Bringing Digital IP Development into the 21st Century	Warren Savage, Prahlad Menon
			Droop! There it is!	Michael Durr
			Accelerating Timing Closure for Network on Chips (NoCs) using Physical Awareness	Andy Nightingale, Guillaume Boillet
IP	Cherished Memories - Exploring the Power of Innovative Memory Architectures for AI Applications	With all the discussion about Moore's Law, one thing is for sure: Memories aren't scaling as much as logic. On the other hand, AI applications, so popular these days, require increasing amount of memory. Add to that the need to extend the use of available fabs, and you get a great reason to explore new memory paradigms. In this session we'll explore cutting-edge technologies transforming the landscape of memory design. The expert speakers will share real-world applications in AI, machine learning, and edge computing, exploring new technologies and optimization strategies.	Samsung's IP QA methodology using Solido Crosscheck	Peter Park, Siddharth Ravikumar
			Cherished Memories - Exploring the Power of Innovative Memory Architectures for AI applications	Moshe Zalcberg, Raul Camposano, Andreas Burg, Gideon Intrater, SUSHIL SUDAM SAKHARE
IP	Leading Edge Digital IP	Digital IP design has to improve rapidly to catch up with the speed and performance requirements for massive compute intensive applications in the AI era. IP designers are exhausting every possible combination to improve power, performance and area efficiency of digital design. In this section, we talk about algorithmic changes that double the throughput of an Ethernet switch, a fast calibration method for PHYs, an FPGA based hardware accelerator, AI based technology library selection to optimize the PPA, arbiter logic for high performing systems and a highly efficient CXL memory compression design for data center applications.	100Gbps class in-vehicle Ethernet Switch architecture for next generation autonomous driving car	Takahiro Sekine
			Hybrid Tiled Vector Systolic Architecture to	Jay Shah, Nanditha Rao
			Evaluating power, performance, and area for standard cell libraries from different IP providers	Aravind Radhakrishnan Nair, Ajay Kumar, Austin Shirley, Lars Kishchuk
			Window Feedback Based Multi-Master Arbiter IP for Efficient Hardware Resource Sharing	Gianluca Rigano
			Open Compute Platform(OCF) ready Hardware Accelerated CXL Memory Compression IP for Data Center Applications	Nilesh Shah

Session Event Types	Session Title	Session Description	Submission Title	Contributors
IP	Methodologies for Streamlining SoC Design Challenges	SoC design poses several challenges in terms of design flow and methodologies. The use of advanced and automated methods is crucial, especially for compute-intensive workloads. This session presents various topics on design methodologies such as: accelerating placement-aware timing closure for NOCs, an open-source design flow promising support for generative AI, accelerating DRC checks, CDC multimode signoff methodology, droop mitigation and scalable sign-off/QA flow.	Advancing Power Signoff for High Speed $\Sigma\Delta$ ADC	Vaibhav Garg, Vaibhav Garg, Paras Garg, Atul Bhargava, Prayes Jain
			Considering Selective Resistance Extraction for Performance & Accuracy Trade-off for Memory IP Simulation	Praveen Kumar Verma, Anuj Dhillon, Harshit Sharma, Vartul Sharma, Rakesh Shenoy, Ashish Kumar
			Fast and Deterministic Memory Yield Estimation Using Machine Learning Augmented Statistical Simulations	Ashish Kumar, Shashank Gupta, Rakesh Shenoy
			Interfacing High-Voltages Directly to Low Power CMOS Process Die for RF, MEMs and Analog Applications	Stephen Fairbanks, Pradeep Thiagarajan, Lih-Jen Hou
IP	NoC NoC - Who's There?	"Network on a Chip" or NoC refers to a communication subsystem that enables communication between various components or modules on the chip. It is a network-based approach to managing data transfer and communication within a microprocessor or a system-on-chip (SoC).	NoC NoC - Who's There?	Moshe Zalcberg, Moshe Zalcberg, Guillaume Boillet, Kamal Desai, Jonathan Ezroni, Andrea Majstorovic
IP	The Open Chiplet Economy and AI	Session Structure The Open Chiplet Economy and AI - A brief introduction of how the open chiplet economy can help with AI, Bapi Vinnakota (OCP), Cliff Grossner (OCP) A Survey of AI-related IP for the Open Chiplet Economy - High performance D2D PHY IP and Other soft IP relevant to AI, Elad Alon (Blue Cheetah) Letizia Giuliano (Alphawave) AI-Related Chiplets in the Open Chiplet Economy - An overview of chiplets relevant to building AI and HPC systems, John Shalf (LBL) + AI Packaging Workflow - Basic and advanced packaging workflows for AI systems, Lihong Cao (ASE) +	The Open Chiplet Economy and AI	Bapi Vinnakota, Bapi Vinnakota, Cliff Grossner, Letizia Giuliano, John Shalf, Lihong Cao, Elad Alon
IP	What's New in IP Verification and Validation?	The increasing complexity of SoC designs, coupled with the high cost of a re-spin due to functional bugs, requires constant innovation in verification techniques and methodologies to ensure first pass silicon success. This session discusses a collection of such techniques spanning automated methods to create simplified test cases for tool bugs, use of symbolic simulation for the verification of interface IP, protocol validation of high speed serial links, power estimation and tracking using real world use cases, fast and efficient methodology for multi-PVT corner validation, and a formal verification framework for DDR5 power management features.	GPU Power Tracking and Optimization Using Emulation	Sandesh Saokar, Veera Dasari, Navid Farazmand
			Automated Design Scenario Extraction From A Large Design For Faster Debug Of Static Verification Tools	Gaurav Pratap, Vishal Keswani, Sachin Bansal, Amit Goldie, Sanjay Gulati
			Watt's Up with DDR5: Formal Verification Framework for Robust DRAM Power Management	Pradip Prajapati, Anshul Jain, Mounica Kothi, Erin Rasmussen, Rocco Salvia
			Beyond Digital: Innovation in symbolic simulator to empower IO analog circuit validation	Pawan Verma, MANISH BANSAL, Anil-kumar Dwivedi, Amandeep Kaur, Hari Sathianathan
			Enabling Protocol Validation of High Speed Serial Links using SerDes to transfer data between PHY Chip and Link layer on FPGA	Priyanka Goel, Aashish Bhide, Vivek Uppal, Ameer Youssef, Nitin Sharma